

スケーラブルな高集積量子誤り訂正システムの開発

Development of Scalable Highly Integrated Quantum Bit Error Correction System

プロジェクトマネージャー 小林和淑（京都工芸繊維大学）

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Kyoto Institute of Technology (KIT), Japan



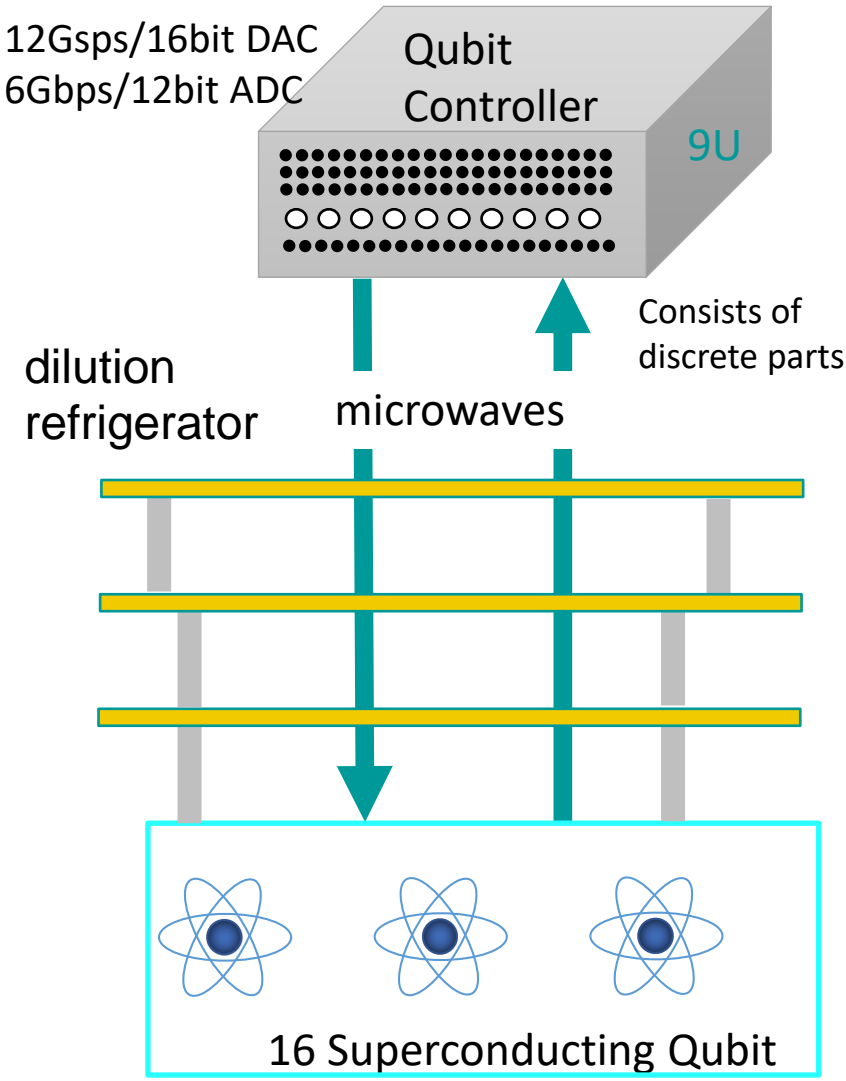
Search “QUBECS”

<https://www.greenlab.kit.ac.jp/qubecs/index.html>

Outline

From NISQ to FTQC

NISQ=Noisy Intermediate-Scale Quantum, FTQC=Fault Tolerant Quantum Computer



Current small-size QC

Backend to correct errors

Frontend qubit controller

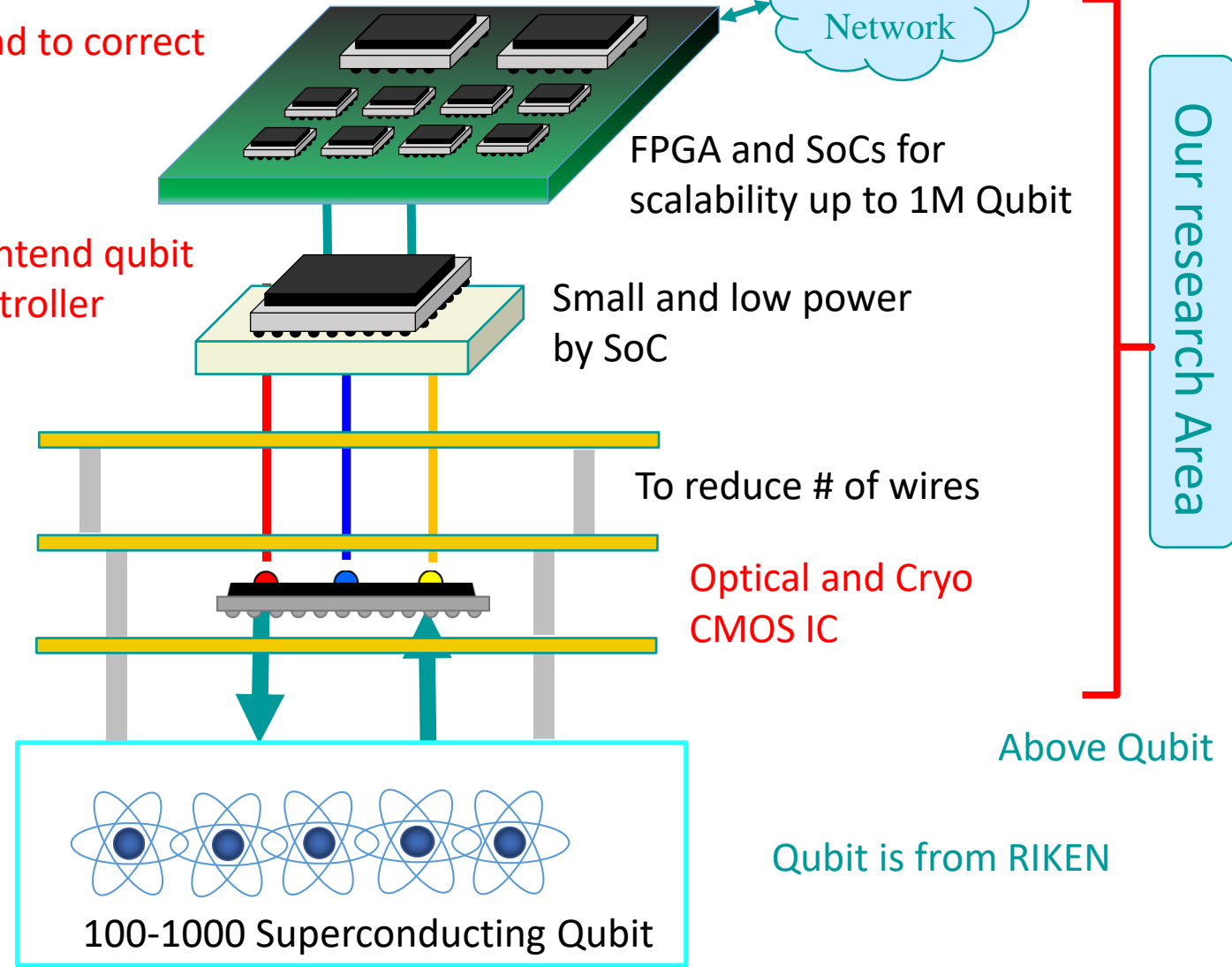
RT

(70K)

3-4K

0.8K

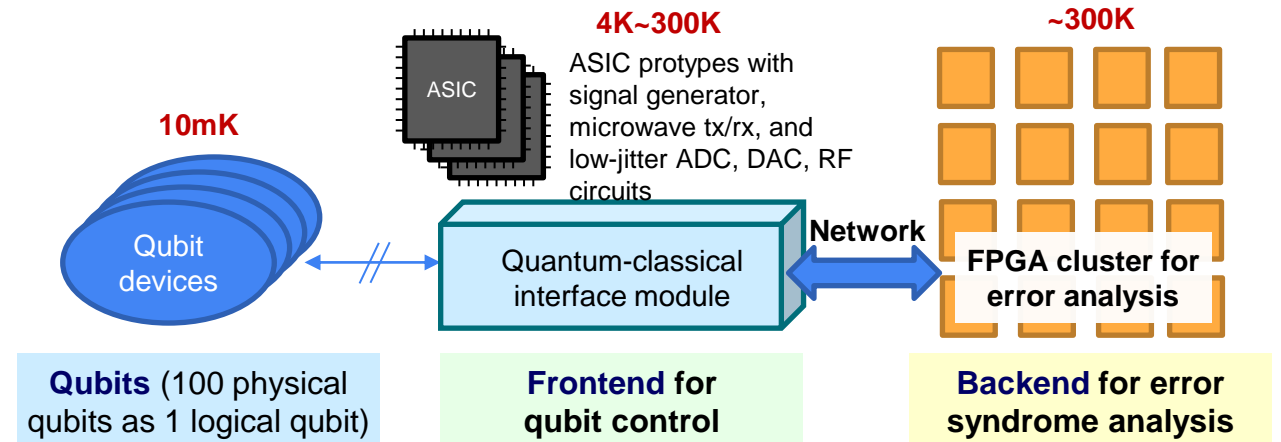
10mK



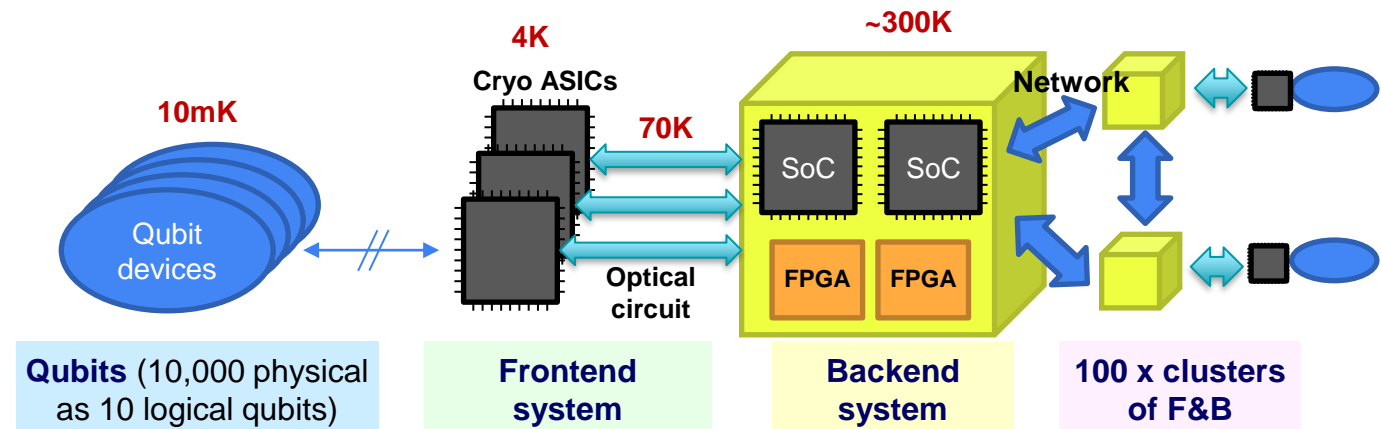
Our targeted scalable QC

Our Goals on 2025 and 2030

- **2025**
 - ✓ Develop a prototype system for FTQC with ~100 physical qubits
- **2030**
 - ✓ Develop a system for FTQC scalable up to 1M physical qubits



2025: Prototype system for FTQC with ~100 physical qubits



2030: System for FTQC scalable up to 1,000,000 physical qubits

Principal Investigators

*: Subject Leader



Dr. Sano*
(RIKEN)



Prof. Kadomoto
(U. Tokyo)



Prof. Osana
(Kumamoto U.)

Subject 1: Backend for error correction



Dr. Miyoshi*
(Quel-inc)

Subject 2: Advanced Qubit
Control Frontend



Quel-1: Qubit controller



Prof. Shiomi*
(Osaka U.)



Prof. Shintani
(KIT)



Prof. Sato
(Kyoto U.)

Subject 3: Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits



Prof. Kobayashi*
(KIT)



Prof. Tsuchiya
(Shiga Pref. U.)



Prof. Takai
(KIT)



Prof. Miyahara
(KEK)

Subject 4: Cryo CMOS ASICs for Frontend/backend

**Subject 5: Frontend ASICs at room temperature
(will be included soon)**

Experts of qubit-controllers, computer architectures and integrated circuits

Qubits from RIKEN vs. IBM vs. Google

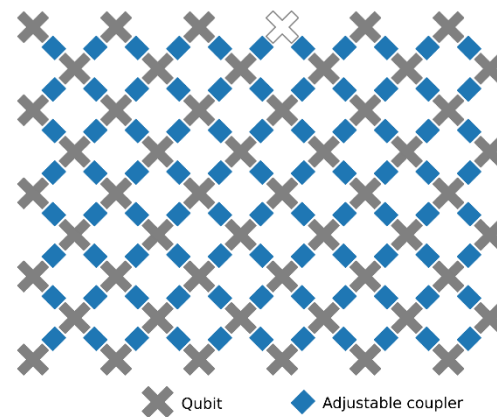
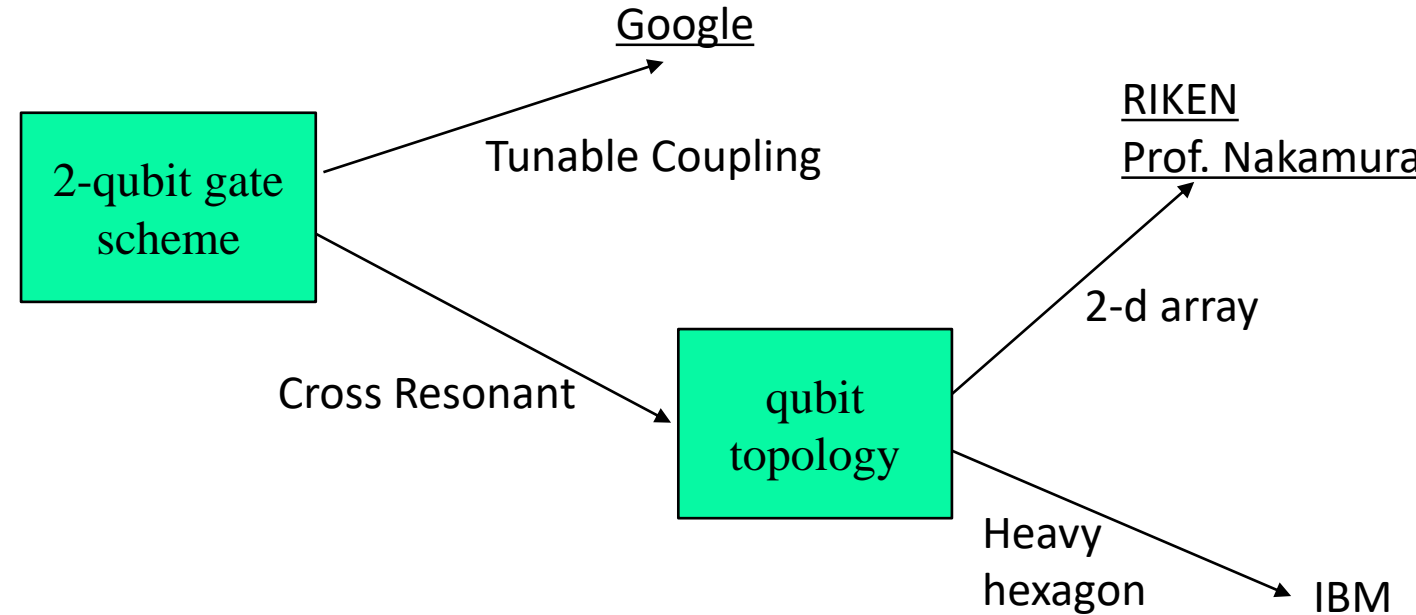
- Our first target is superconducting qubit from RIKEN

- 2-qubit gate scheme

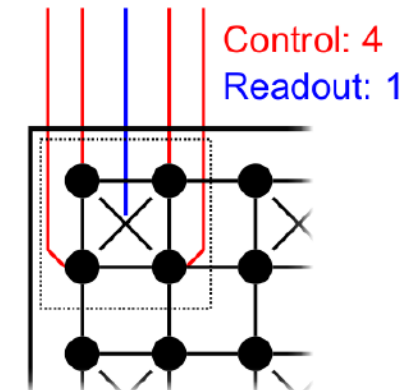
- ✓ Cross resonance gate – RIKEN, IBM
- ✓ Tunable coupling – Google

- Qubit topology

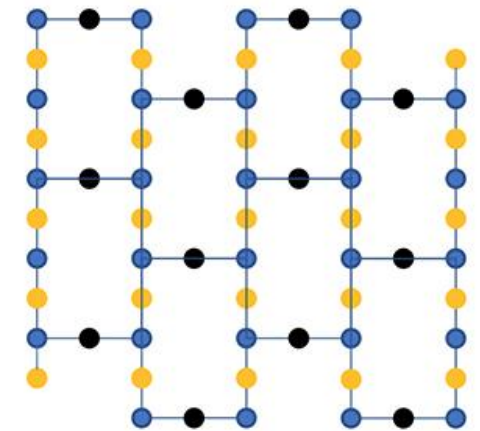
- ✓ 2-d array - RIKEN, Google
- ✓ Heavy hexagon - IBM



Google*



RIKEN Prof. Nakamura ***



IBM**

*<https://arstechnica.com/science/2019/10/inside-googles-quantum-computing-efforts/>

**<https://www.ibm.com/blogs/research/2020/09/hardware-aware-quantum/>

*** Shuhei TAMATE et al. "Toward realization of scalable packaging and wiring for large-scale superconducting quantum computers,"

IEICE Transactions on Electronics, Article ID 2021SEP0007

Subject 1: Backend for Error Correction

Theme 1: Scalable backend system for error correction by Dr. Sano

Theme 2: ASIC implementation of QEC cores by Prof. Kadomoto

Theme 3: Dependable error correction backend by Prof. Osana

Subject 1: Backend for Error Correction

- **Overview**

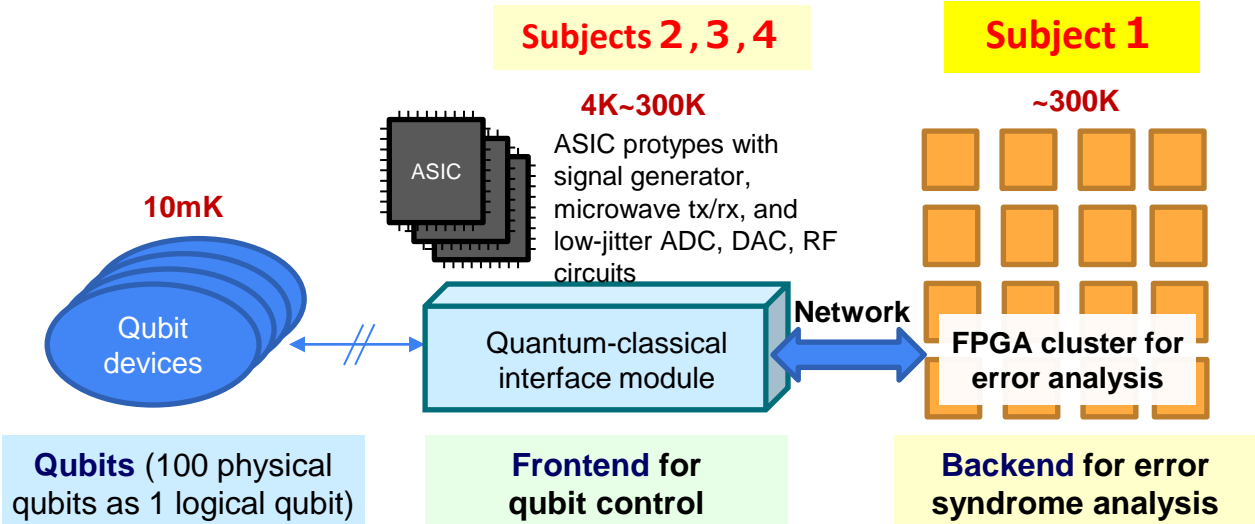
- ✓ Develop a backend system for error correction scalable to 1M physical qubits

- **Research Target**

- ✓ Prototype a backend system for qubit error correction
- ✓ Demonstrate error syndrome analysis on a scale of 100s of physical qubits at an acceptable throughput and latency
- ✓ Show scalability for more physical qubits

- **R&D themes**

- ✓ **Theme 1** (RIKEN)
Scalable backend system for error correction
- ✓ **Theme 2** (The University of Tokyo)
Error correction algorithm for ASIC-based backend system
- ✓ **Theme 3** (University of the Ryukyus)
Dependable error correction backend



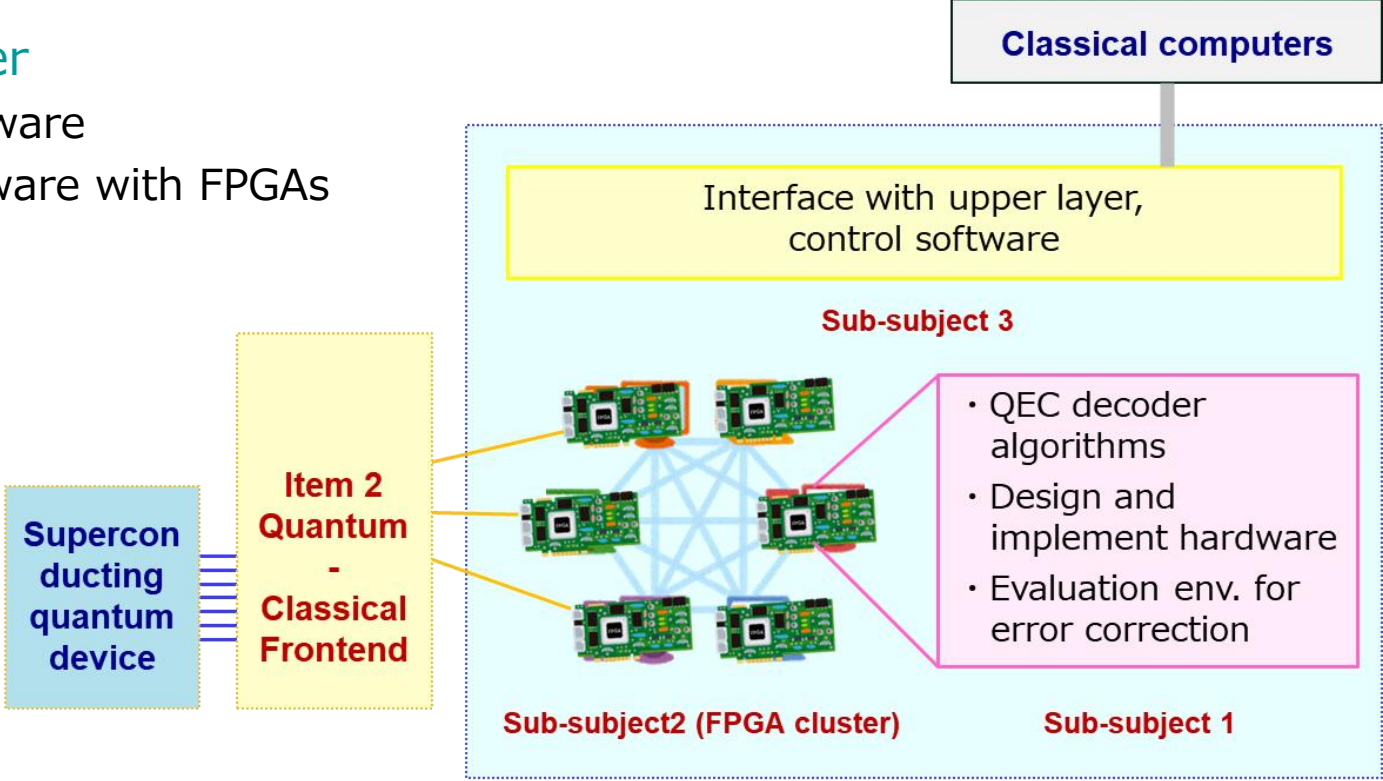
Expected system for FTQC with 100 physical qubits

Theme 1 : Scalable Backend System for Error Correction



Dr. Sano
(RIKEN)

- **Goal**
 - ✓ Proof-of-concept of scalable QEC with FPGA-based backend system prototype
- **R&D sub-themes**
 - ✓ **Sub-theme 1:**
Algorithm and hardware for QEC decoder
 - Develop QEC decoder algorithms for hardware
 - Design and implement QEC decoder hardware with FPGAs
 - ✓ **Sub-theme 2:**
FPGA cluster for backend system
 - ✓ **Sub-theme 3:**
Interface with upper layer and system architecture



Subject 1 Theme 1: Scalable backend system for error correction

Theme 1 : Progress

- **Algorithm and hardware for QEC decoder**

- ✓ Survey QEC decoder algorithms
- ✓ Identify promising one for hardware, Union find (UF) decoder
 - Lower latency, higher scalability
 - acceptable accuracy close to MWPM
- ✓ Propose systolic-array for UF, and evaluate it by software-based emulation
- ✓ Submit a paper to Q-CASA workshop

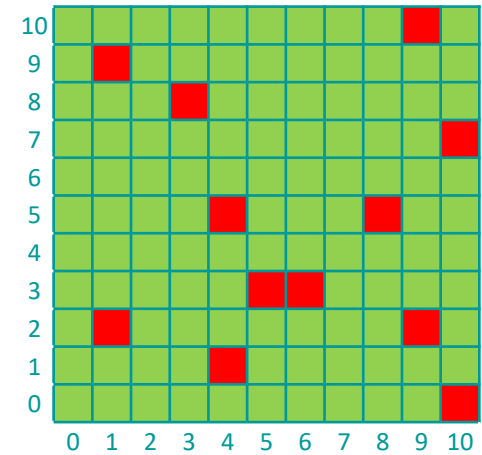
N. Delfosse et.al, Quantum 5, 595, 2021

- **FPGA cluster for backend system**

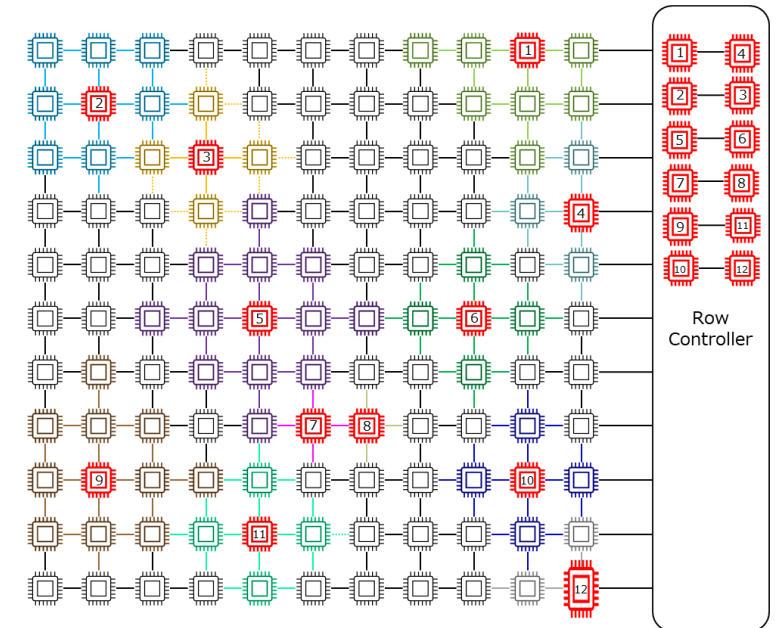
- ✓ Design and prototype Shell (system-on-chip) for FPGA
- ✓ Start considering specification of FPGA cluster for the backend

- **Interface with upper layer and system architecture**

- ✓ Survey existing interfaces



Model graph of 2D ancillary qubits



Concept of systolic array for UF

Theme 2 : ASIC Implementation of QEC Cores

- **Goal**

- ✓ Highly-integrated low-power ASIC-based QEC core for scalability

- **R&D sub-themes**

- ✓ **Sub-theme 1:** Design of ASIC-based QEC architecture

- Design QEC core architecture and construct a system by connecting a prototype ASIC chip and the FPGA cluster

- ✓ **Sub-theme 2:** Performance evaluation of ASIC-based QEC core

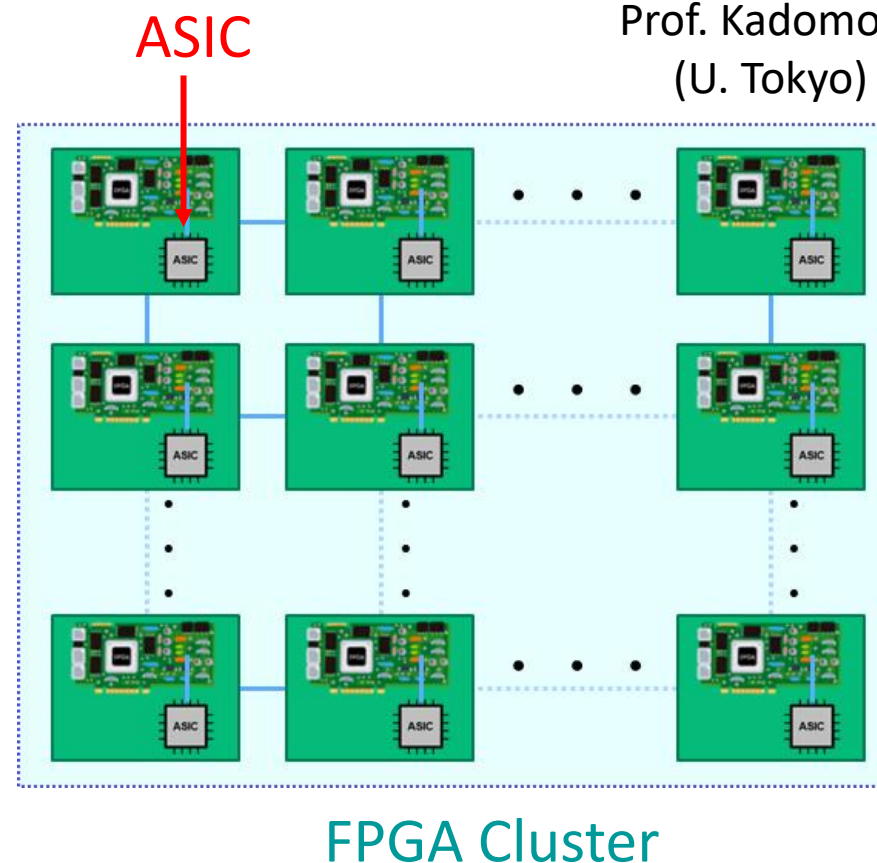
- Evaluate the performance through simulation, and demonstrate improvement of the overall system performance

- ✓ **Sub-theme 3:** Development of QEC TEG chip

- Implement each functional block of the QEC core as an ASIC and verify the performance improvement through measurements



Prof. Kadomoto
(U. Tokyo)



Theme 2 : Progress and Plans

- **Set up ASIC design/simulation environment**
 - ✓ 28-nm CMOS technology
- **Survey on the various components of QEC backend**
- **Developed some QEC decoders in HDL**
 - ✓ Greedy decoder Y. Suzuki, et al. IEEE Micro, 2022 1110-1125
 - ✓ Union-Find (UF) decoder N. Delfosse et.al, Quantum 5, 595, 2021
- **Near-term milestones**
 - ✓ Evaluate the decoders through RTL simulations in ASIC technologies (28, 7-nm CMOS)
 - ✓ Prepare the design environment for TEG chip 1 (22-nm CMOS)

Theme3: Dependable Error Correction Backend

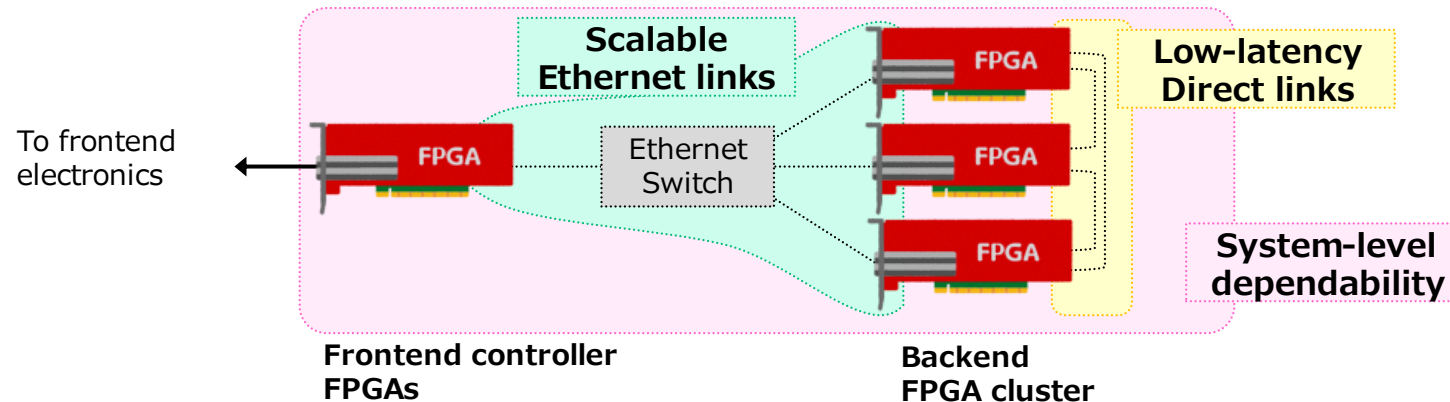
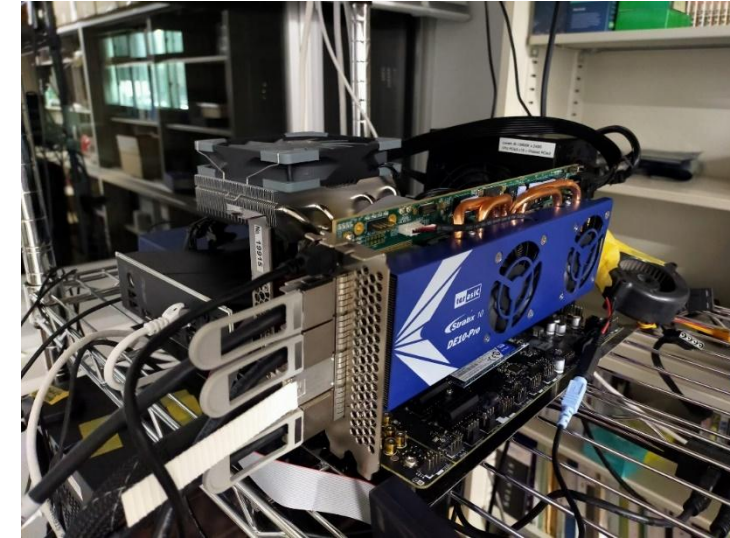


Prof. Osana
(Kumamoto U.)

- **Interconnection network for the backend FPGA cluster**
 - ✓ Intra-backend and backend-frontend interconnect
 - Scalable option: 100 Gbps Ethernet
 - Low-latency option: 100+ Gbps direct links
 - ✓ Development & evaluation on a mock-up

Dependability of FPGA clusters

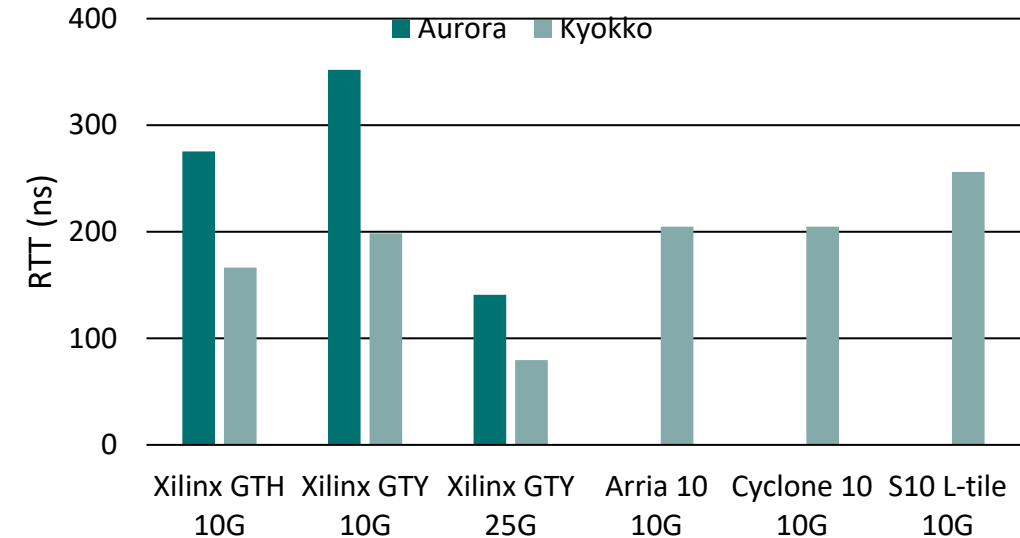
- ✓ Investigate SEU (Single Event Upset) and other dependability problems on large-scale FPGA clusters



Interconnect for FPGA clusters



- **Error correction within a few μs**
 - ✓ To fit within gate operation period
 - ✓ FPGA processing latency + interconnect latency
 - Ethernet switch has too much latency ~ 700 ns
 - ✓ Low-latency interconnect is crucial
- **Developing Kyokko**
 - ✓ Xilinx Aurora 64b66b compatible, 100 Gbps capable
 - ✓ Fits with both the frontend (Xilinx) and backend (Intel)
 - ✓ Reliability features are scheduled in 2023
- **Towards the ultra low-latency interconnect**
 - ✓ Less than 100 ns latency with Xilinx GTY
 - ✓ Agilex version for RIKEN FPGA cluster in 2023



RTT: Round Trip Time

Subject 2: Advanced Qubit Control Frontend

By Dr. Miyoshi

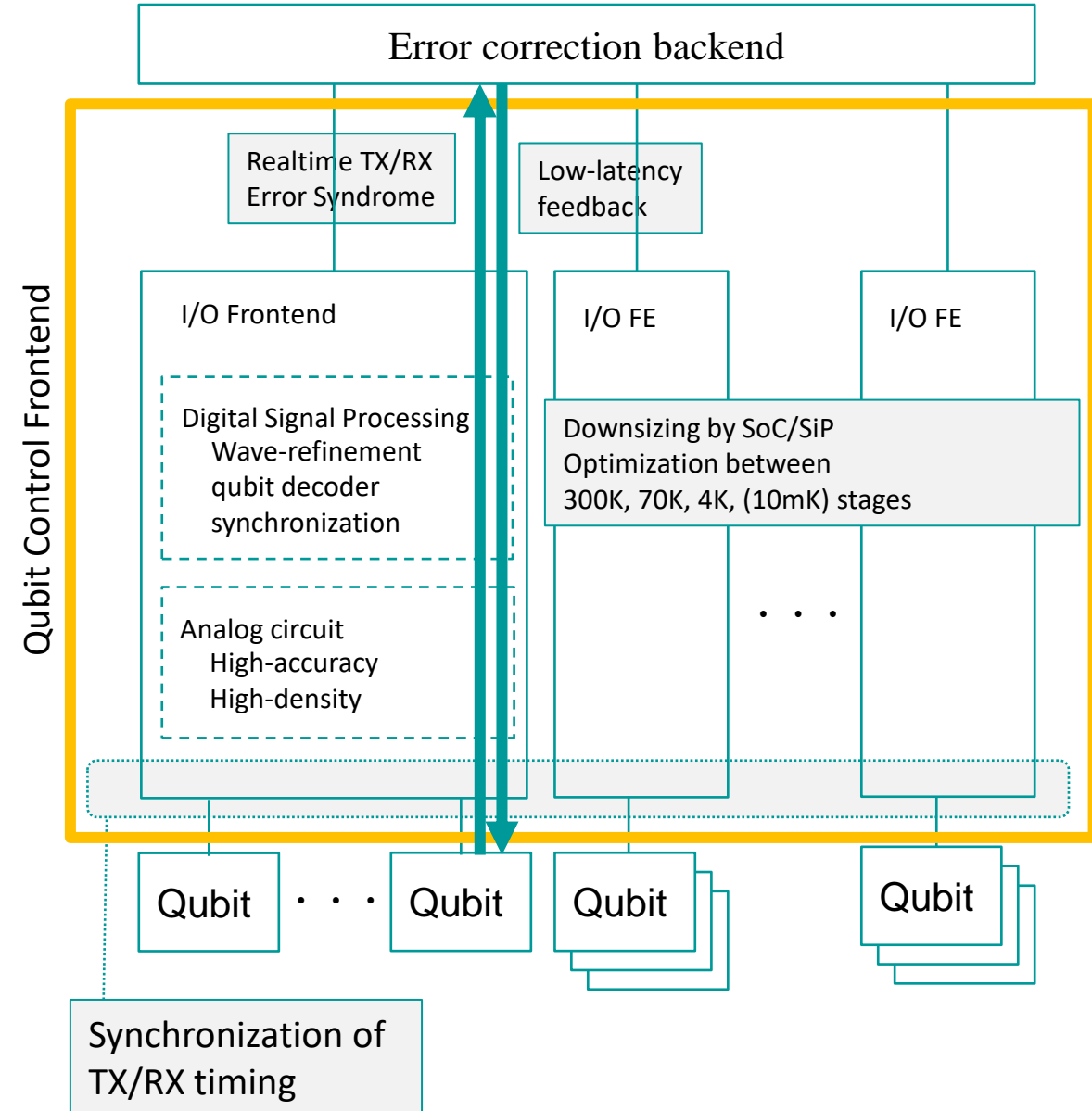


Dr. Miyoshi*
(Quel-inc)

Subject 2 Goal

- **Goal: Establish the qubit control and **measurement** frontend system**
 - ✓ Realtime TX/RX qubit data b/w frontend-backend
 - ✓ Highly-accurate signal transmission
 - ✓ Synchronization for scalability
- **Issues**
 - ✓ Signal quality and stability
 - ✓ How to synchronize
 - ✓ Efficient connection with backend
 - Low-latency feedback
 - Optimized data scatter/gather
 - ✓ Downsizing (Currently 9 U/4 qubit)
 - ✓ Optimization in 300K, 70K, 3-4K, (10mK)

w/ Prof. Osana



Downsizing by SoC/SiP

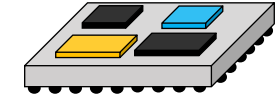


9-10GHz, 20GHz RF frontend:
Downsizing by combining a component supports multiple I/Os.

Analog Mixer for RF:
Downsizing by packing modules as a SiP

FPGA and AD/DA chips:
Downsizing by packing modules as a SoM

Power management and drivers for temperature control:
Downsizing by adoption lightweight temperature control



SiP (System in a Package)

Totally downsizing for much more qubit control/measurement

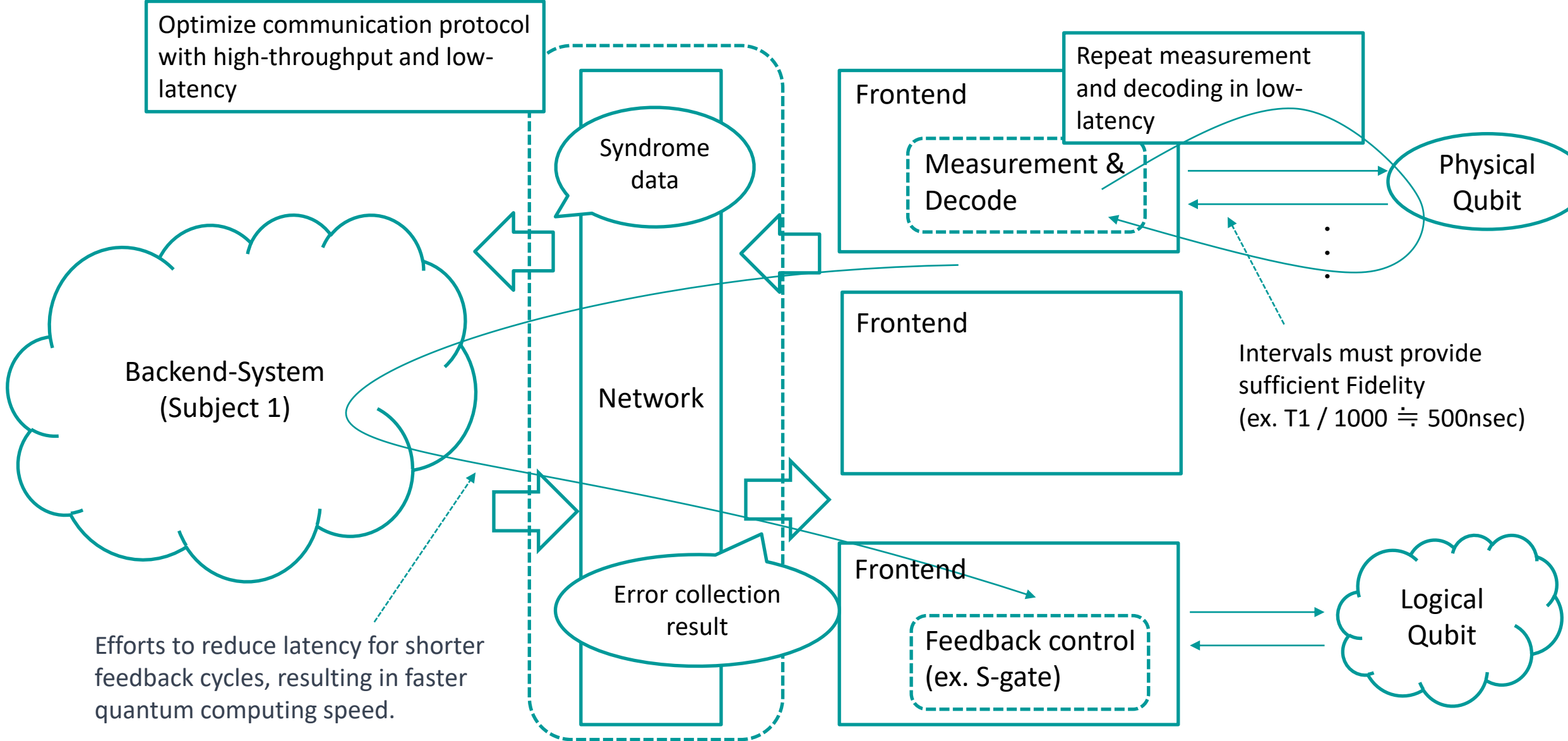


SoM (System on a Module)

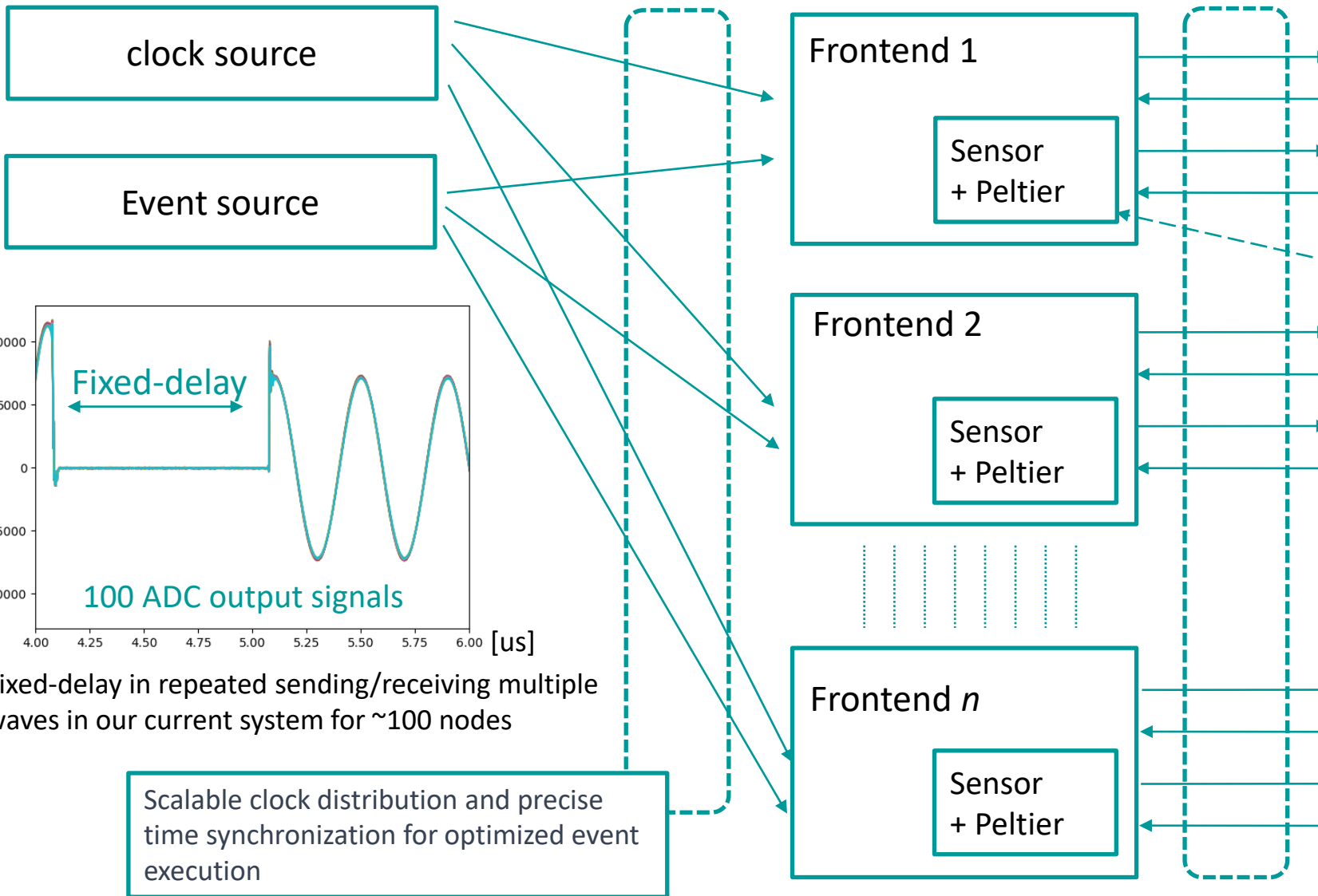
<https://japan.xilinx.com/products/som/what-is-a-som.html>

Our current system for 4-Qubit control/measurement

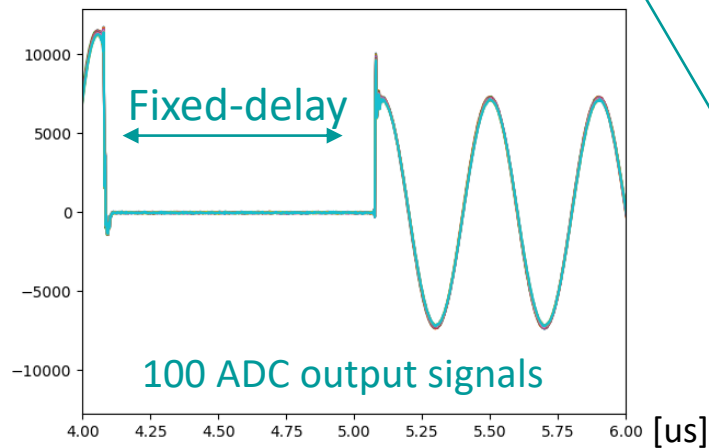
Control/Measurement Qubit for FTQC



Highly-accurate synchronous signal processing

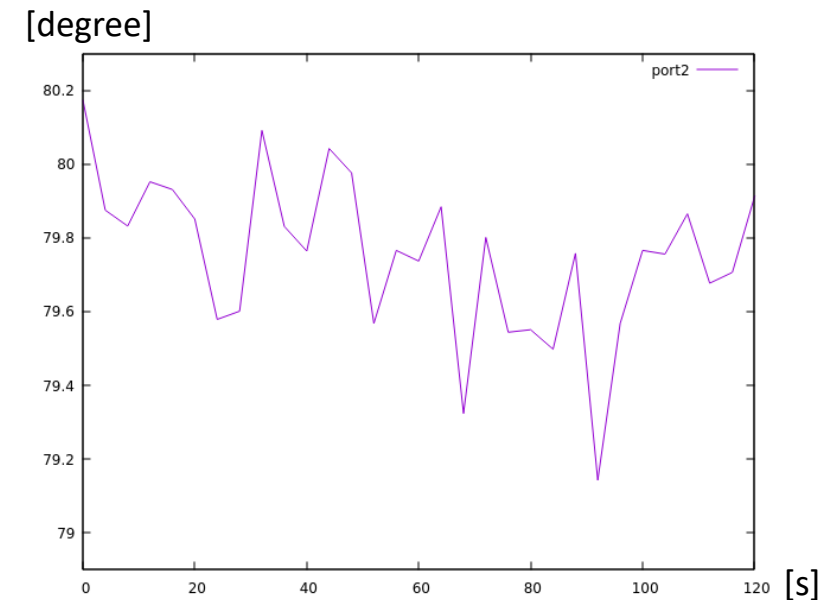


- ✓ Suppress phase fluctuation for each microwave TX
- ✓ Optimization for wave-figure for individual qubit



Fixed-delay in repeated sending/receiving multiple waves in our current system for ~100 nodes

Scalable clock distribution and precise time synchronization for optimized event execution



Current system achieves fluctuation of 2.5 deg. RMS in 120 sec. with temperature control

Subject 3: Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits

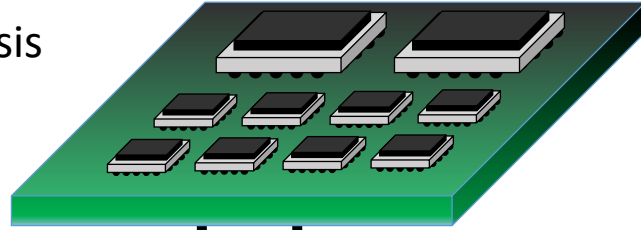
Theme 1: Exploring photonic integrated circuits operating in the extremely low-temperature environment by Prof. Shiomi

Theme 2: Development of transistor model for Si CMOS devices in the extremely low-temperature range of 4K to 70K by Prof. Shintani

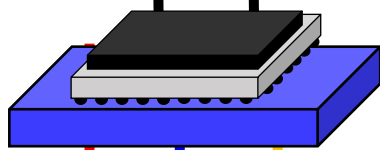
Theme 3: Cryo-CMOS integrated circuits with extremely low power consumption by Prof. Sato

Subject 3 Goal

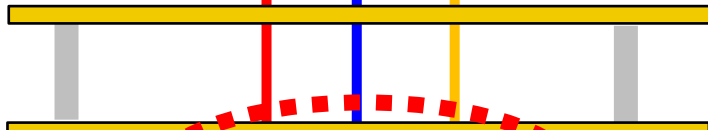
Syndrome Analysis



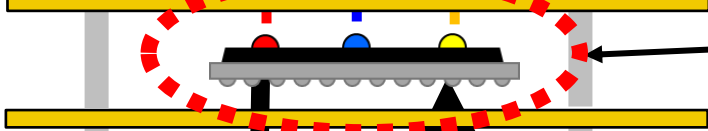
RT Frontend



(70K)



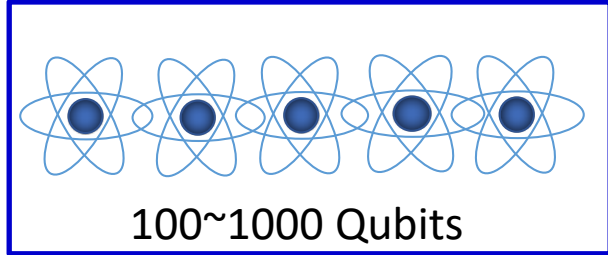
4K



0.8K

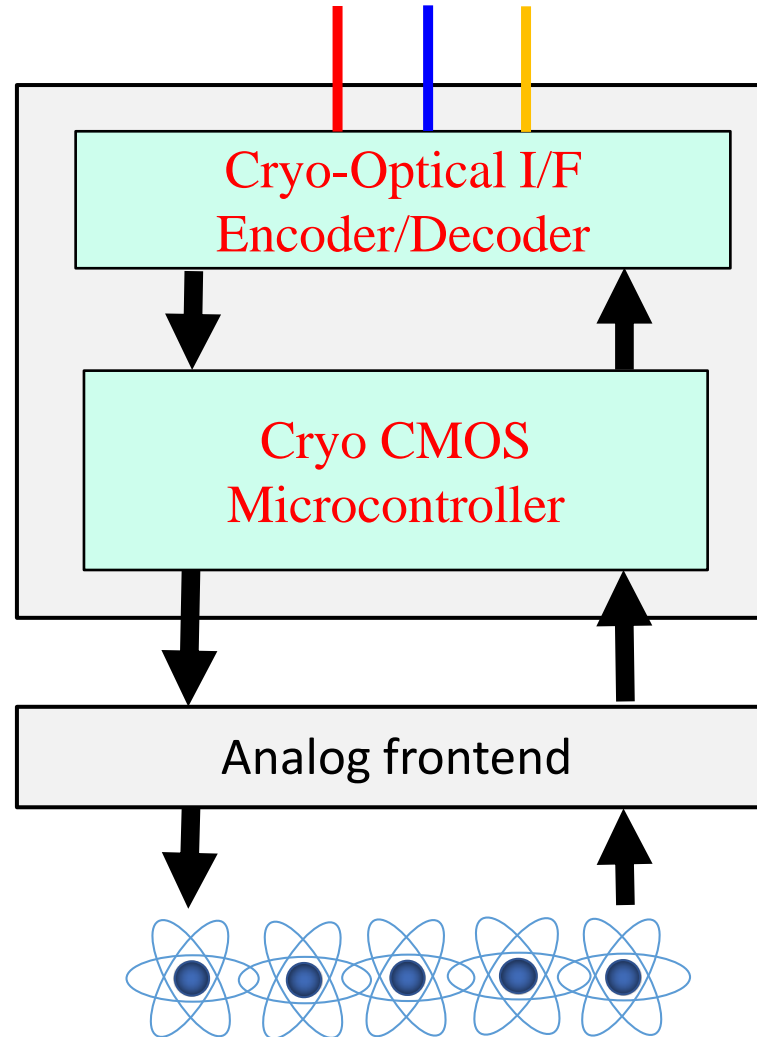


10mK



Quantum Computer Overview

✓ Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits



Performance optimization by Cryo PDK

Theme 1: Exploring photonic integrated circuits operating in the extremely low-temperature environment

• Cryo-Optical I/F

✓ Milestone

- 2022 Measurement at cryogenic environment
- 2023 Optical device measurement and characterization
- 2024-2025 Modeling and prototype design

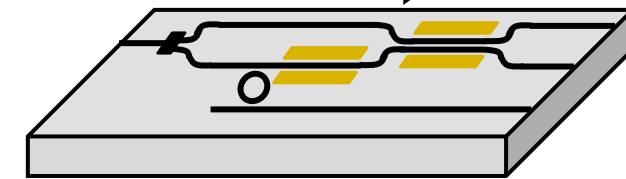
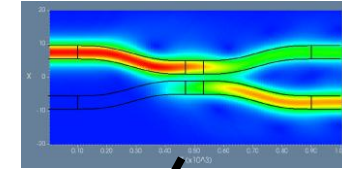
✓ Challenges

- Optical HW architecture for Photonic/Cryo-CMOS Integrated Circuits
- Design methodology for optical-electronical encoder/decoder design

• Progress

- ✓ Prototype chip design
- ✓ Measurement setup for cryogenic environment
 - Progress explanation at next page

Analysis & Modeling

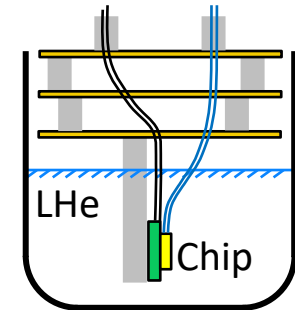


Chip fabrication and Measurement



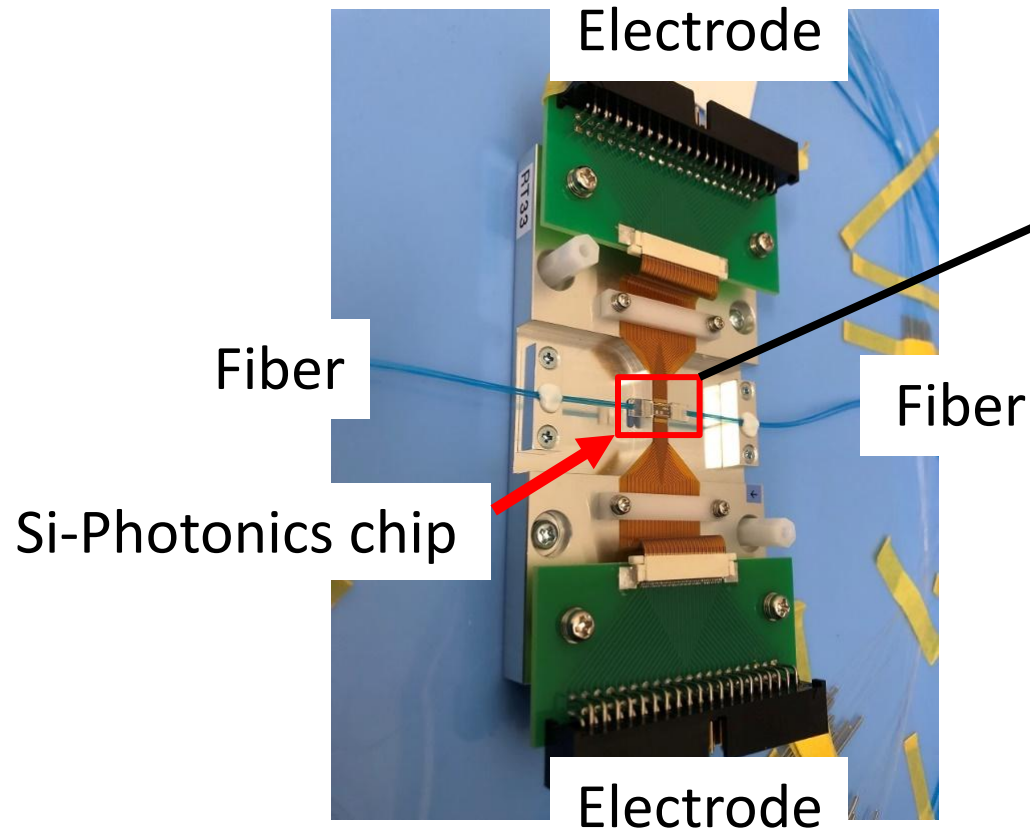
Prof. Shiomi*
(Osaka U.)

Electrode Fiber

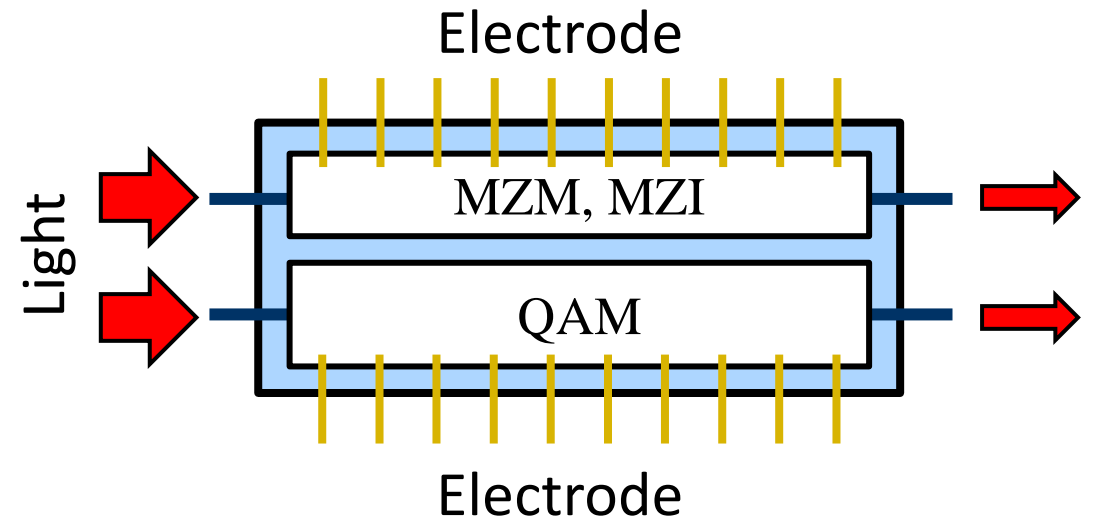


Cryo Environment Measurement

Progress of Theme 1: Prototype chip design



Partial circuit design (TO @ 2023 Feb.)



30 GHz BW @ room temp.

→ To do: how fast at cryogenic temp.?

Future work: Characterization at **cryogenic environment**

Theme 2: Cryo CMOS PDK Development



Prof. Shintani
(KIT)

• Cryo CMOS PDK development

✓ Milestone

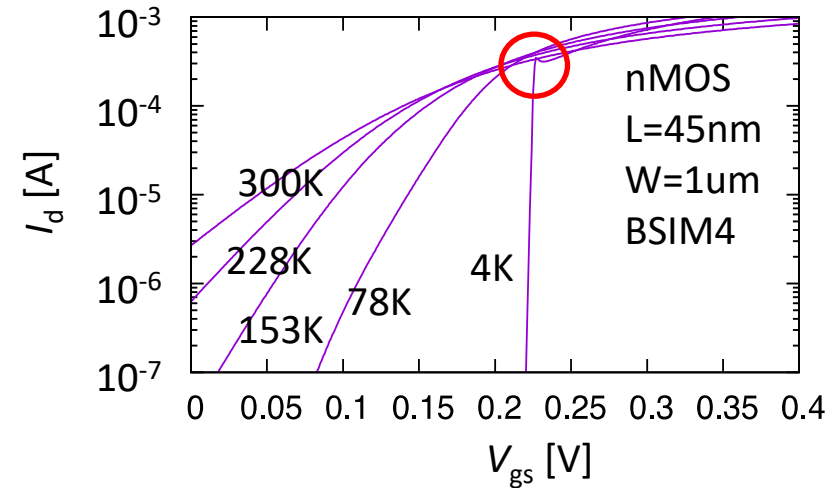
- 2022: Measurement at cryogenic environment
- 2023: Alpha version development (CryoPDK_v1)
- 2024~2025: Alpha version release
Modeling non-ideal characteristics, such as process variation and self-heating effect

✓ Challenges

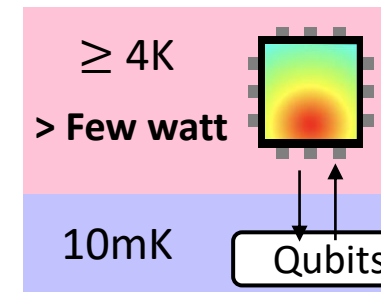
- Development of a **new** Tr. model that can reproduce the characteristics at 4K
- Incorporation of physical phenomena that is not considered in industry standard model

• Progress

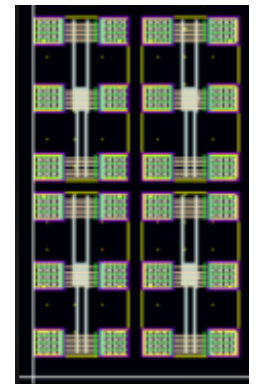
- ✓ Designed 65nm Tr. Array TEG using a CMOS circuit prototype (Jan. T.O.)



Discontinuous effect observed in industrial model



Self-heating effect



Tr. array TEG

Theme 3: Cryo-CMOS Design Platform

• Cryo-CMOS Design Platform

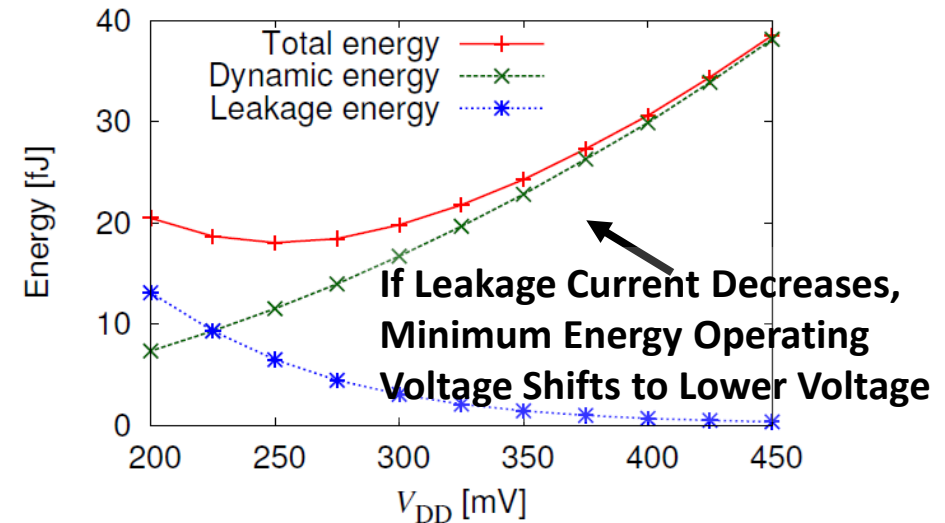
✓ Milestone

- 2022 exploration and implementation of measurement methods for cryogenic temperature environments
- 2023 prototype, measure, and model basic circuit blocks such as flip-flops, SRAMs, PLLs for operation at cryogenic temperatures
- 2024-2025 optimize and minimize power consumption of circuits for cryogenic applications

✓ Challenges

- Reduction of 'dynamic power' that remains mostly unchanged even in extremely low temperatures
- Exploration of circuit paradigms specialized for cryogenic temperature, focusing on ultra-low-leakage-current **dynamic** circuits

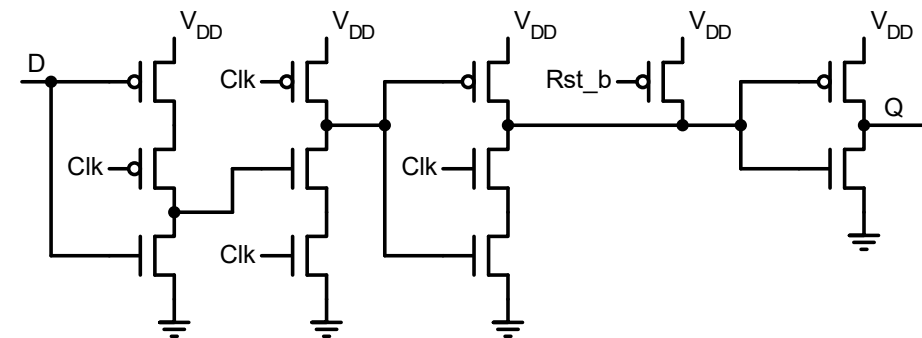
Energy Consumption of RO Circuit at 300K



Prof. Sato
(Kyoto U.)



Prof. Awano
(Kyoto U.)

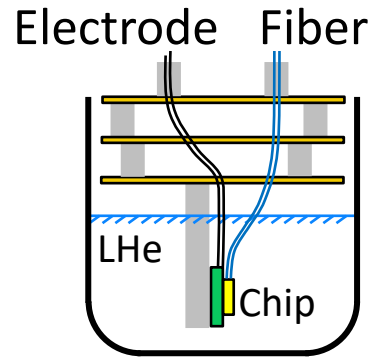


Dynamic DFF w/o clkb

Setups for Cryo Measurement Environments

- **Optical circuit @ Osaka Univ.**

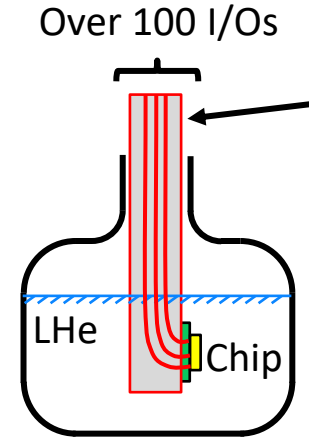
- ✓ Cryogenic environment



- Cryo dewar design for photonic chip
- Prototype delivered in 2023 Summer

- **Digital CMOS circuits @ Kyoto Univ.**

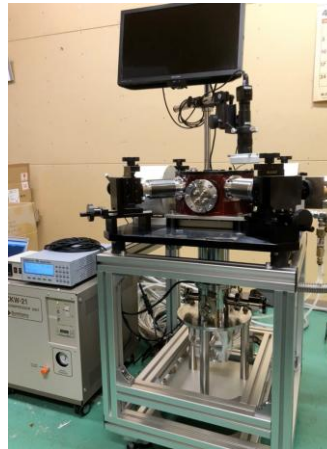
- ✓ Cryogenic environment



- Rod design for cryogenic dewar
- Over 100 I/Os

- **Analog CMOS circuits @ KIT**

- ✓ LHe circulating type prober
- ✓ 10K to room temperature
- ✓ Connect to B1500 (Keysight)



- ✓ Cryocooler-based environment

- Temperature can be changed from 4K to room temperature
- ~24 I/Os.

Subject 4: Cryo CMOS ASICs for Frontend/backend

**Theme 1: Digital circuit implementation and reliability enhancement techniques
by Prof. Kobayashi**

Theme 2: RF front-end circuit by Prof. Tsuchiya

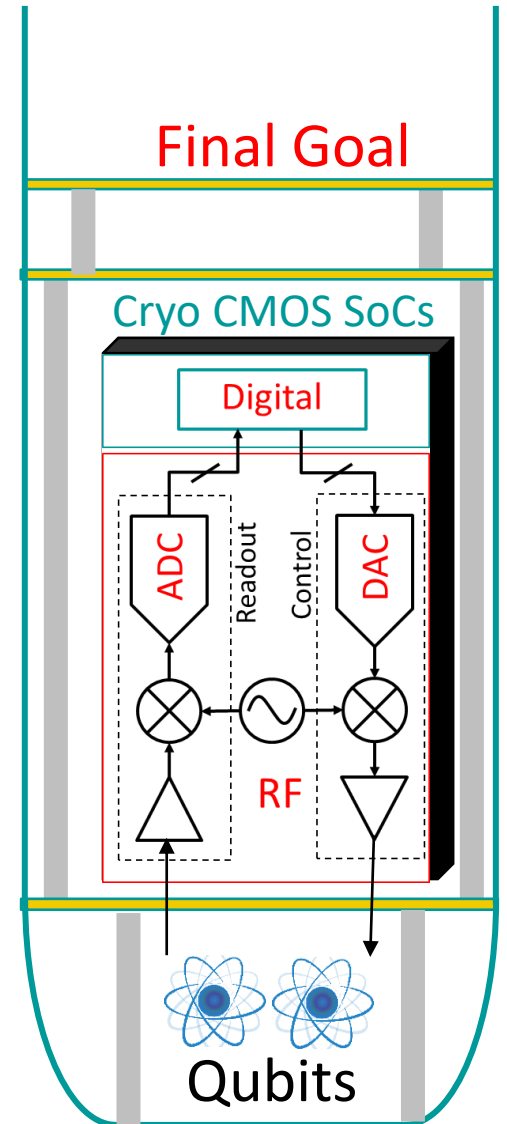
Theme 3: High-speed DAC for frontend by Prof. Takai

Theme 4: High speed ADC for frontend by Prof. Miyahara

Subject 4: Cryo CMOS ASICs for Frontend/backend

- **Goal:** To implement ASICs operating at a cryogenic temperature to control qubits (Frontend) and to correct errors (Backend)
- **Research items**
 - ✓ **Digital** circuit implementation and reliability enhancement techniques (Prof. Kobayashi, KIT, Japan)
 - ✓ **RF** frontend circuit (Prof. Tsuchiya, Shiga Pref. Univ., Japan)
 - ✓ High-speed **DAC** for front-end (Prof. Takai, KIT, Japan)
 - ✓ High speed **ADC** for front end (Prof. Miyahara, KEK, Japan)
- Fabrication process will be a 22nm bulk CMOS (Scaled from 28 nm)
 - ✓ High-performance and cost-effective! 2mmx3mm chip can be fabricated by around a few M JPY.
 - ✓ 28nm bulk is used by many research projects such as Google.

3K-4K



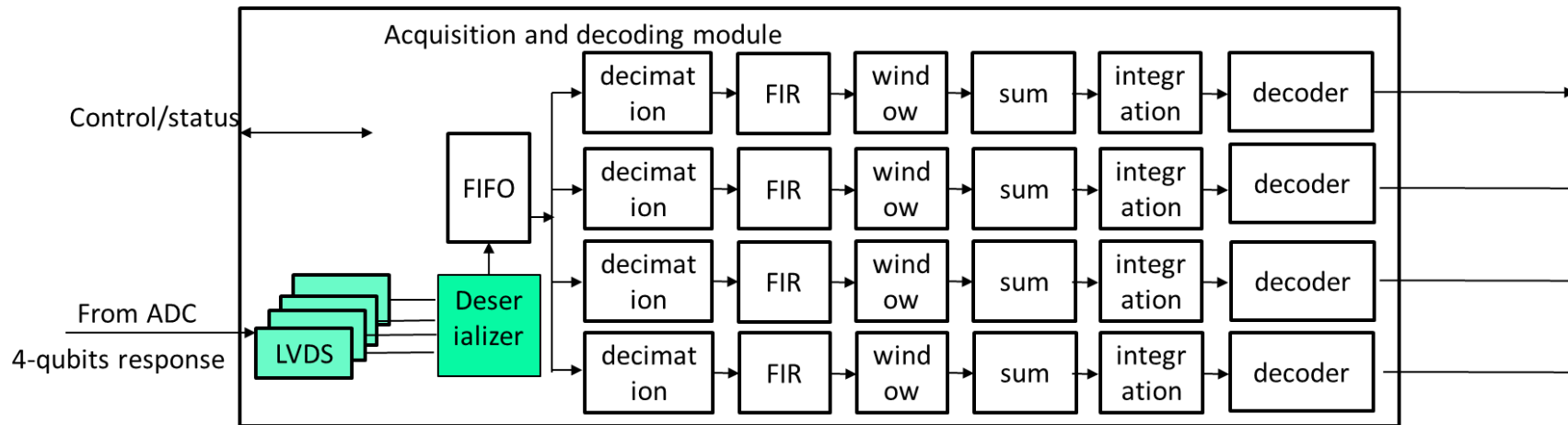
Theme 1: Digital circuit implementation and reliability enhancement techniques



Prof. Kobayashi*
(KIT)

• For frontend

- ✓ Migrate FPGA-based design by Quel (Miyoshi) to ASIC
 - Not easy-going. Synchronous reset on FPGA vs Asynchronous reset on ASIC. IP on FPGAs must be replaced by random logics.
 - LVDS interface from qubit by Prof. Miyahara



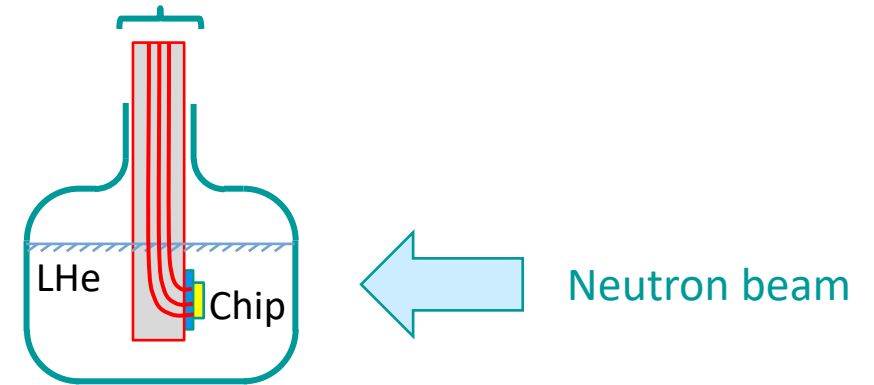
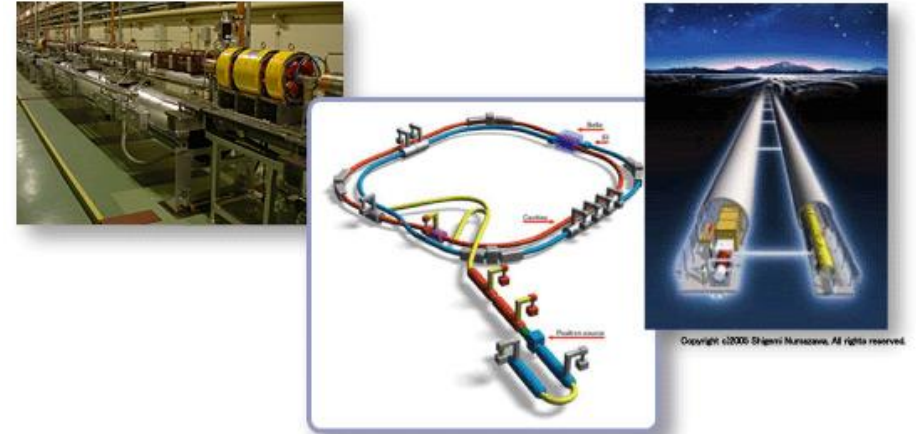
• For backend

- ✓ Implementing an error correction decoder to an FPGA using the HLS code by Dr. Suzuki [1]

[1] Y. Suzuki, et al. IEEE Micro, 2022 1110-1125

Reliability Enhancement

- **FTQC w/ 1M qubit will be similar to a particle accelerator**
 - ✓ Huge classical electronics must be operated with high fidelity
- **Reliability issues must be considered**
 - ✓ Qubit suffer from cosmic ray (by muon) [1, 2]
 - ✓ Classical computers also suffer from cosmic ray (mainly by neutron).
 - Super computers must mitigate soft errors [2]
 - ✓ Will conduct soft error measurement at cryo temperature.



Soft error measurement at Cryo environment in 2023-2024

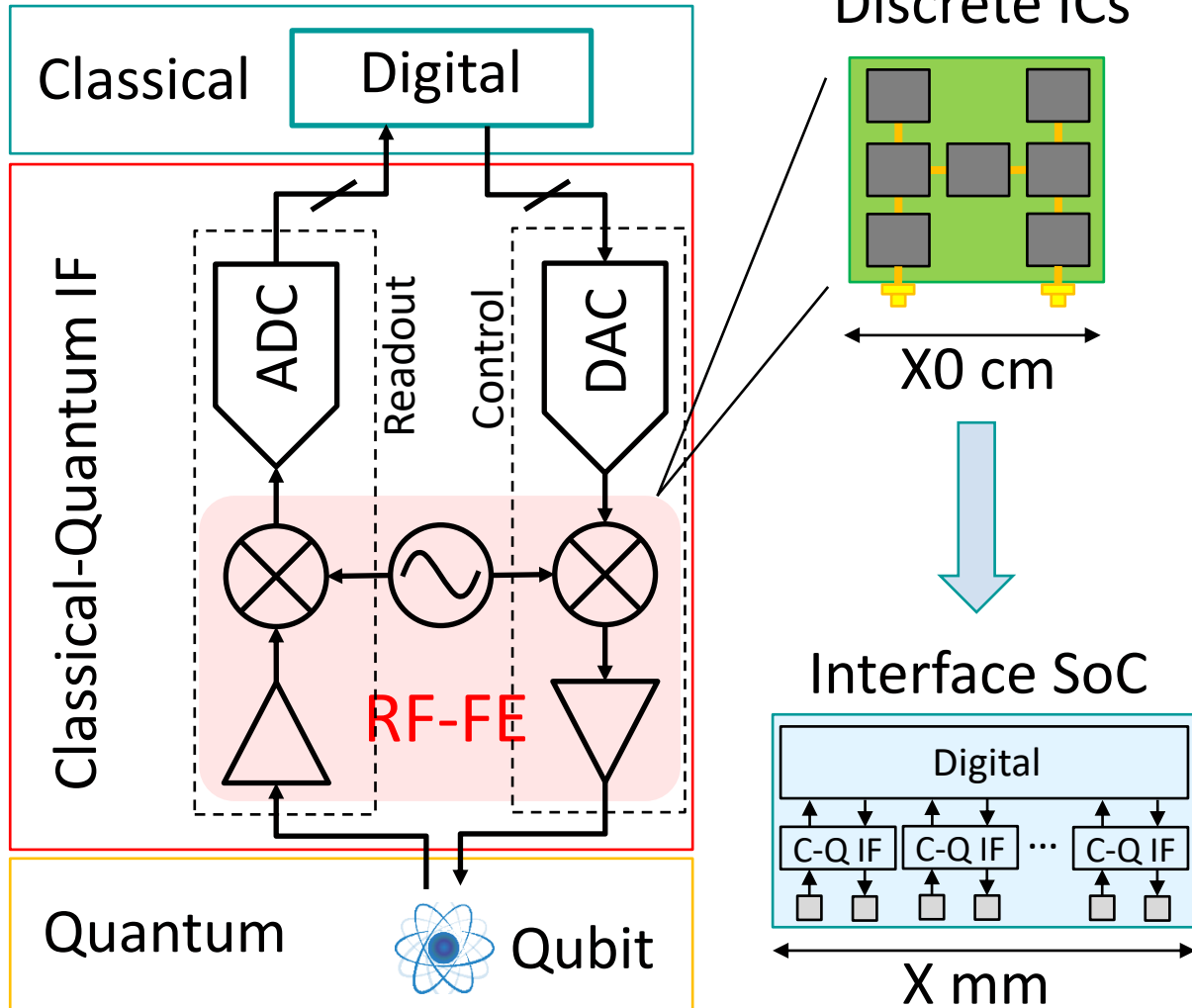
[1] "Q3DE: A fault-tolerant quantum computer architecture for multi-bit burst errors by cosmic rays", by Y. Suzuki et.al, Micro-55, 2022
[2] "Suppressing quantum errors by scaling a surface code logical qubit," Google Quantum AI, Nature 614, 676–681, 2023
[3] "Predicting the number of fatal soft errors in Los Alamos national laboratory's ASC Q supercomputer," S. E. Michalak et.al., TDMR, vol. 5, no. 3, 2005

Theme 2: RF Frontend Circuit



Prof. Tsuchiya
(Shiga Pref. U.)

Goal: Establish Cryo- and RF-CMOS design for RF frontend



Current implementation:

large board, many wires ... **NOT-scalable**

Challenges:

- ✓ Proper cryo- (4K) and RF- (~20GHz) PDK
- ✓ Low-power PLL and mixer
- ✓ Isolation technique among blocks
- ✓ New architecture for scalability toward 1M qubits

Long-term goal:

SoC in cryogenic environment

Milestones

- **Current status**

- ✓ Design basic block (e.g.: PLL) for various operating frequencies

- **Cryo-CMOS RF PDK**

- ✓ High frequency characteristics at 4K, including passives (resistor, inductor, capacitor)
- ✓ Challenges: measurement scheme and physical modeling
 - Special behavior in cryo and RF, ex. anomalous skin effect
- ✓ **Output: Establish RF circuit design environment at 4K**

- **RF frontend circuits for scalability**

- ✓ 10 GHz, <10 mW RF to meet 4K power budget
- ✓ **Output: Provide silicon-proven IPs of element circuits**
- ✓ Challenges: extremely low-power and high-isolation circuit/architecture

Theme3: Automatic Design/Synthesis of D/A Converter

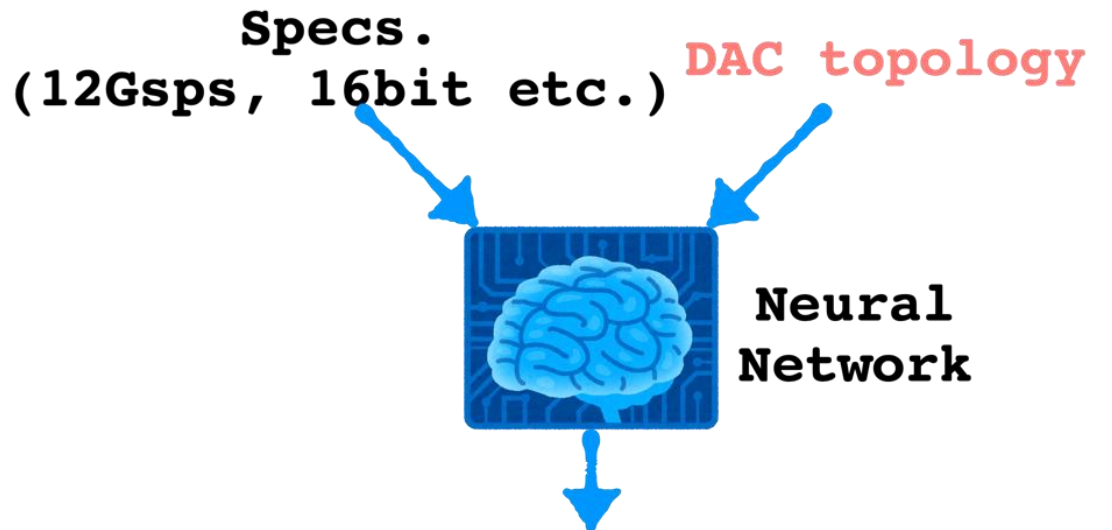


Prof. Takai
(KIT)

Goal

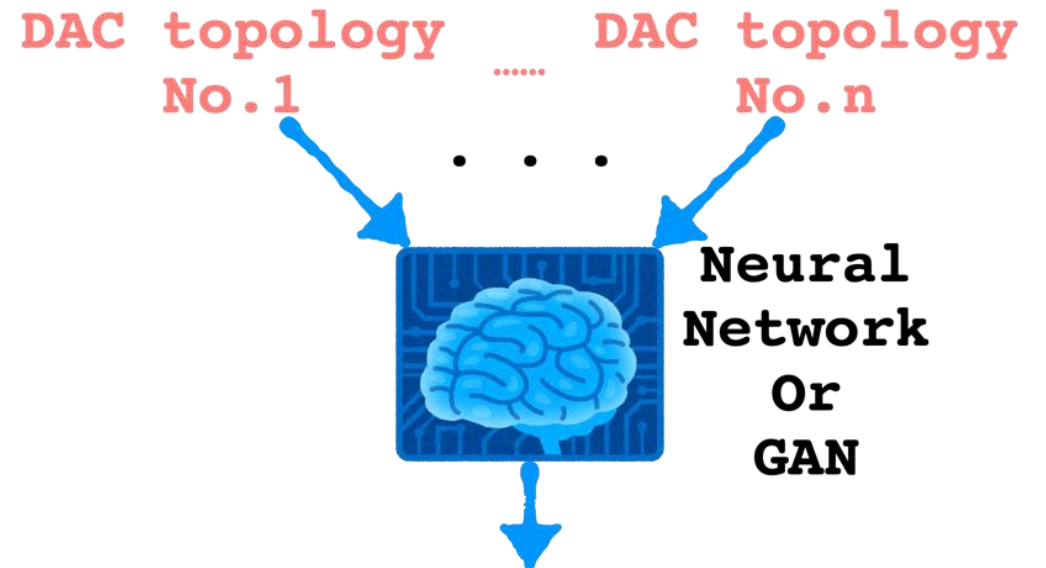
Explore an appropriate architecture for low-power/high-speed/small-area DAC by the **automatic** design/synthesis of the element circuit of DAC under **cryo** environments.

- Automatic **Design** of DAC



Automatically design parameters of DAC to meet the specs.

- Automatic **Synthesis** of DAC



Synthesize New DAC topology

GAN: Generative Adversarial Network

Automatic Design/Synthesis of D/A Converter

Milestone

2022: Building simulation, machine learning and DAC evaluation environment.

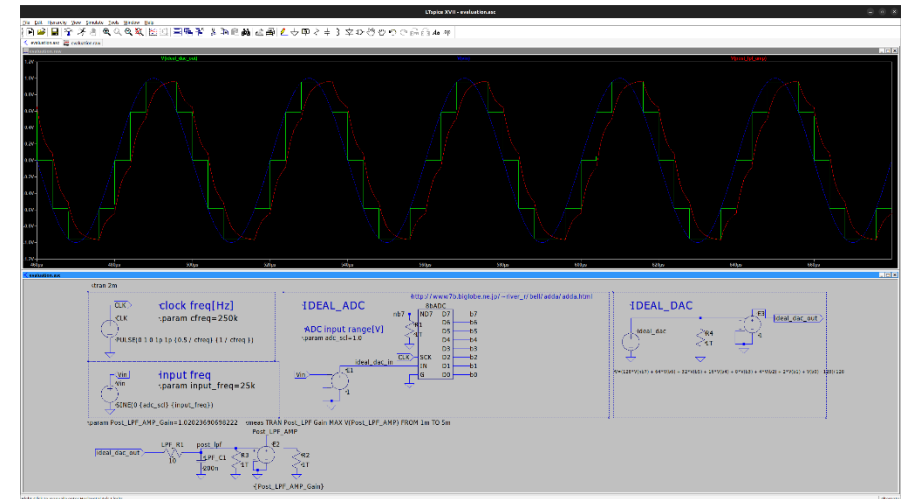
2023: Automatic design of DAC and verification of its operation through fabrication.

2024: Automatic design of high-speed DAC and operation verification through IC.

2025: Automatic design/synthesis of high-speed and high-resolution DAC and verification of its operation through IC.

Progress

- Built an environment of high-speed simulation, machine learning using GPU, and DAC circuit evaluation.
- Training data are collected for automatic design.



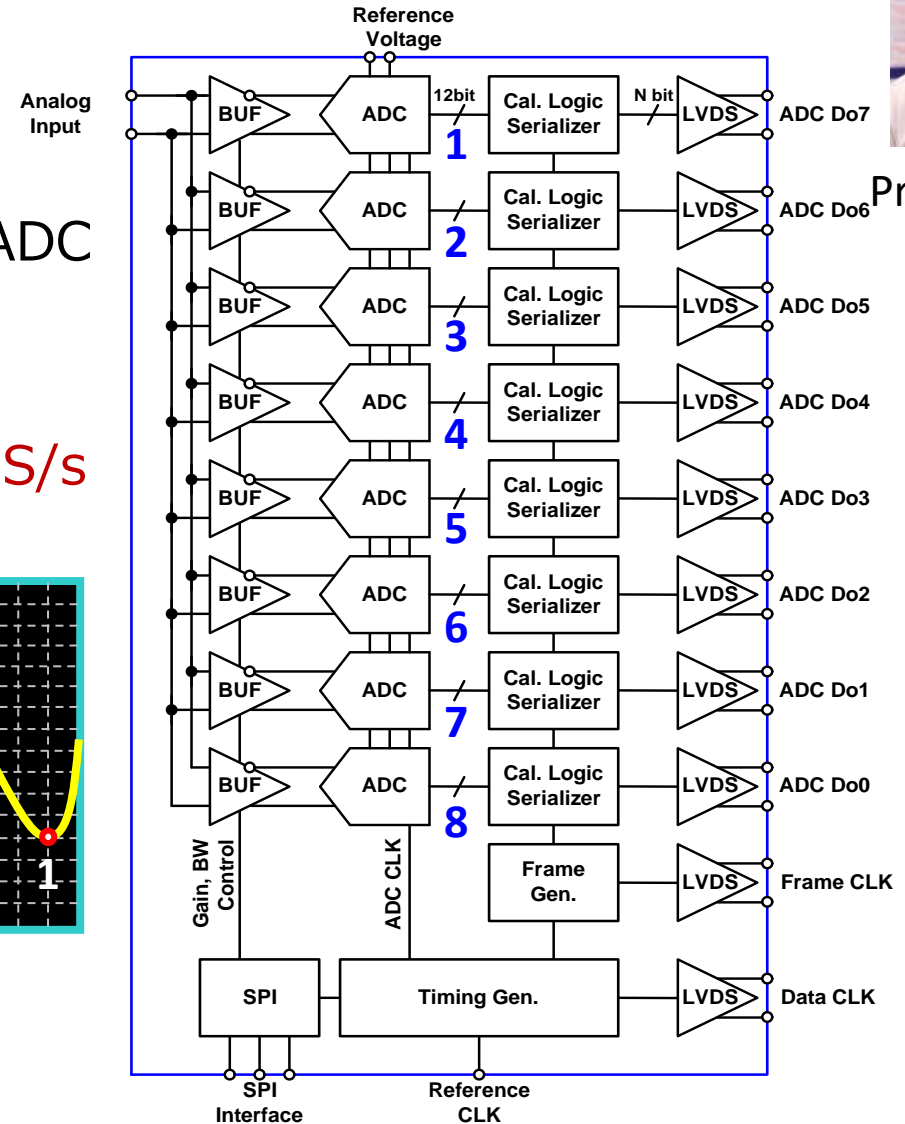
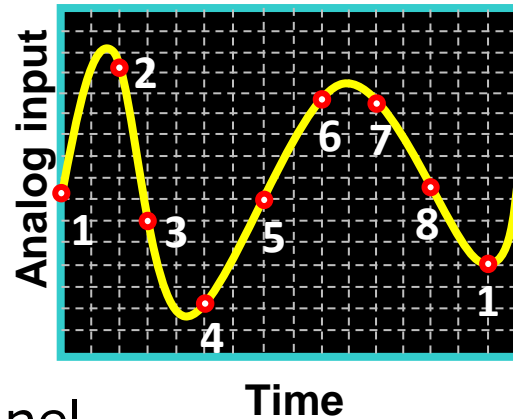
Theme 4: High speed ADC for frontend

● Milestone

- ✓ 2022: Development of evaluation environment
- ✓ 2023: Development and evaluation of a single ADC operating at up to **12 bits, 1 GS/s**
- ✓ 2024-2025: Development and evaluation of an interleaving ADC operating at up to **12 bits, 6 GS/s**

● Challenges

- ✓ Development of scalable ADC architecture suitable for interleaved operation
- ✓ Development of calibration techniques for channel-to-channel mismatches with flexibility



Time-interleaved ADC (8x)



Prof. Miyahara (KEK)

Progress status

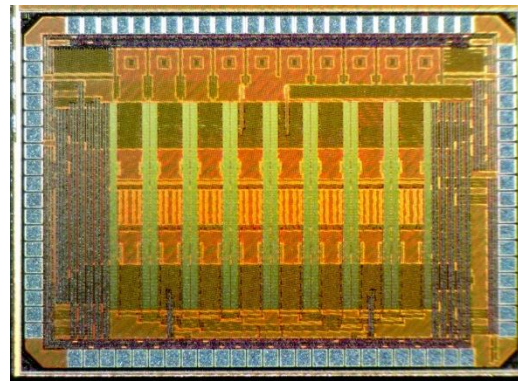
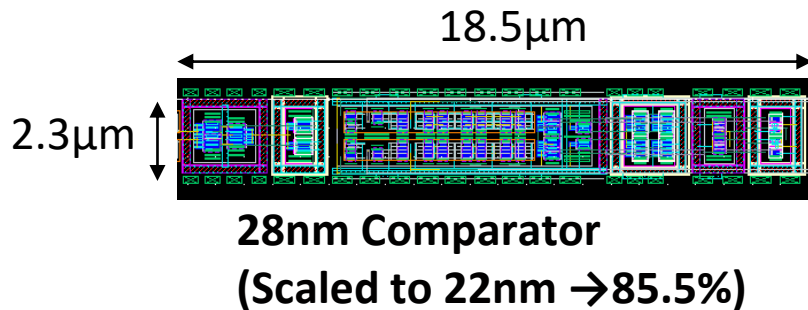
- **Development of ADC and measurement environment**

- ✓ Measurement environment

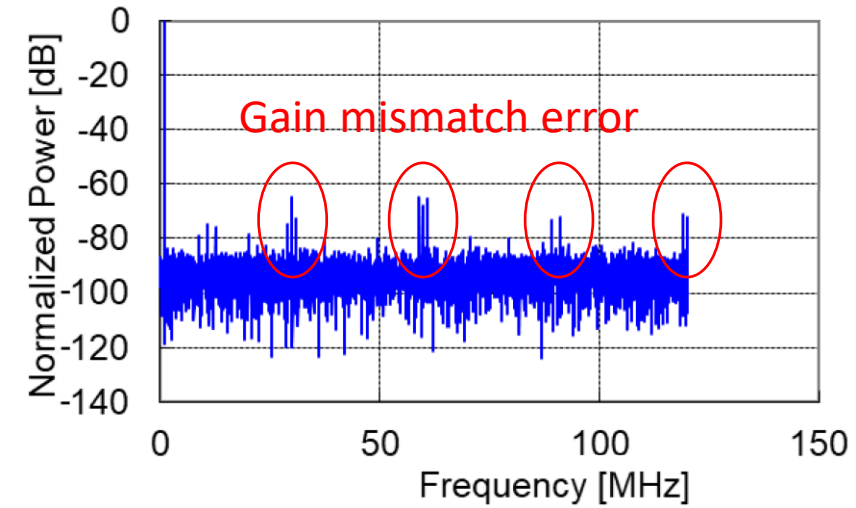
- Installation of low noise analog and clock signal generators
- Investigation of measurement system in Cryo environment

- ✓ Circuit design

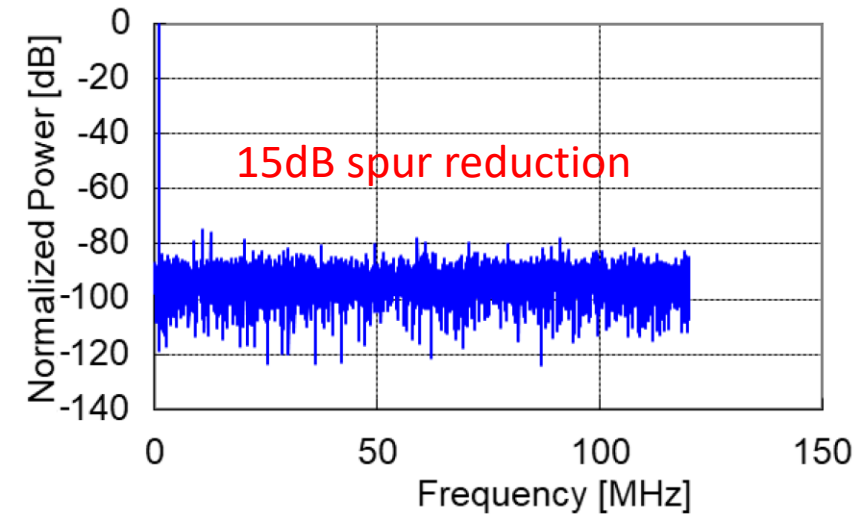
- Investigation of ADC conversion schemes for interleaving
- Investigation of calibration method using downscaling model
- Circuit block design using 28/22nm PDK



Downscaling interleaved ADC
10bit, 125MS/s×8ch=1GS/s



Without calibration



With calibration

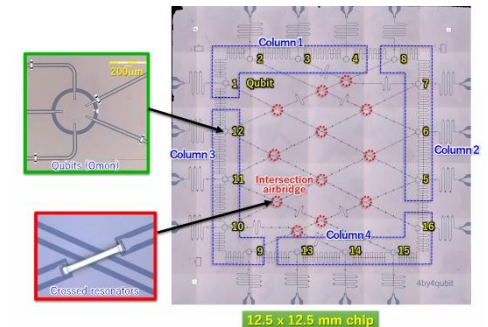
Mismatch calibration

Summary

- **Our project “QUBECS” aims to develop an FTQC with 1 M physical qubits.**
 - ✓ All upper layers above qubit are our targets: from error correction to qubit control
 - ✓ Current target is superconducting qubit from RIKEN
- **11(+1) PIs for these 4(+1) subjects (research topics)**
 - ✓ Subject 1: Scalable error correction system (Backend)
 - ✓ Subject 2: Qubit Controller (Frontend)
 - ✓ Subject 3: Photonic/Cryo-CMOS Integrated Circuits
 - ✓ Subject 4: Cryo CMOS ASICs for Frontend/Backend
 - ✓ **Subject 5: CMOS ASICs for Frontend at Room Temp. (will join soon)**



RIKEN Quantum Computer



RIKEN superconducting qubit

<https://rqc.riken.jp/en/>