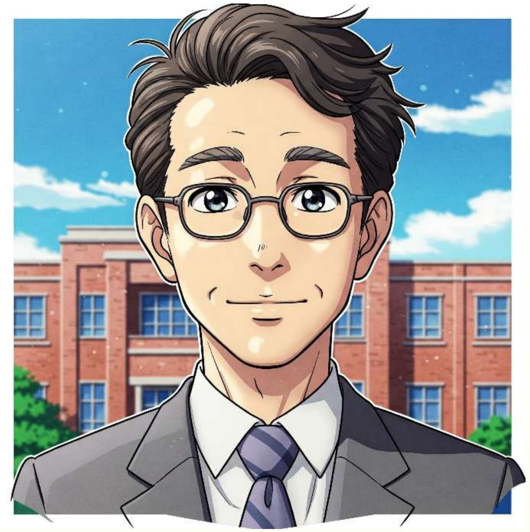
MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

QUBECS
Quantum Bit Error Correction System
Moonshot Target 6



Generated by Gemini

Cryogenic CMOS to Control Quantum Bits (Qubits)

Cool chips 28 on 2025/4/17

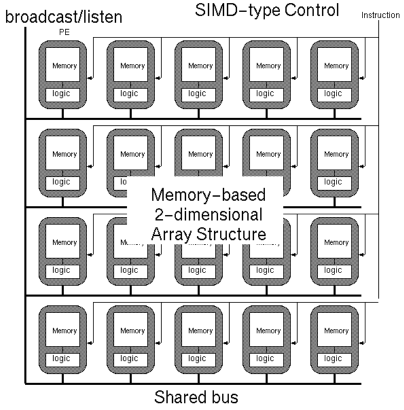
Prof. Kazutoshi Kobayashi

Project Manager of Moonshot Goal 6 (for Fault-Tolerant QC)

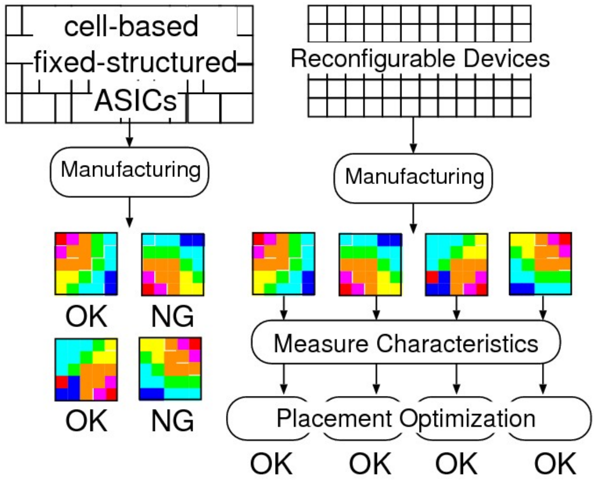
Kyoto Institute of Technology (KIT), Japan

My Research History

- **Compute in Memory (CiM) (1991-2000)**
  - ✓ FMPP (Functional Memory-type Parallel Processor)
    - ➢ CAM (Content Addressable Memory) + Arithmetic Operation
- **System-level Design (2002-2006)**
  - ✓ Resource-shared VLIW for lower-power/higher efficiency
  - ✓ SystemC-based Design
- **Variation-aware FPGA (2004-2009)**
  - ✓ Reconfigure FPGAs by using process variations
- **Reliability Issues from 2007**
  - ✓ Variations, temporal errors (soft errors, RTN), aging degradation (BTI)
- **Power Electronics from 2012**
  - ✓ Gate drivers for SiC, GaN IC
- **Quantum Computer from 2022**
  - ✓ Classical electronics (integrated circuits) to control qubits and correct errors on qubits



FMPP



Variation-aware FPGA

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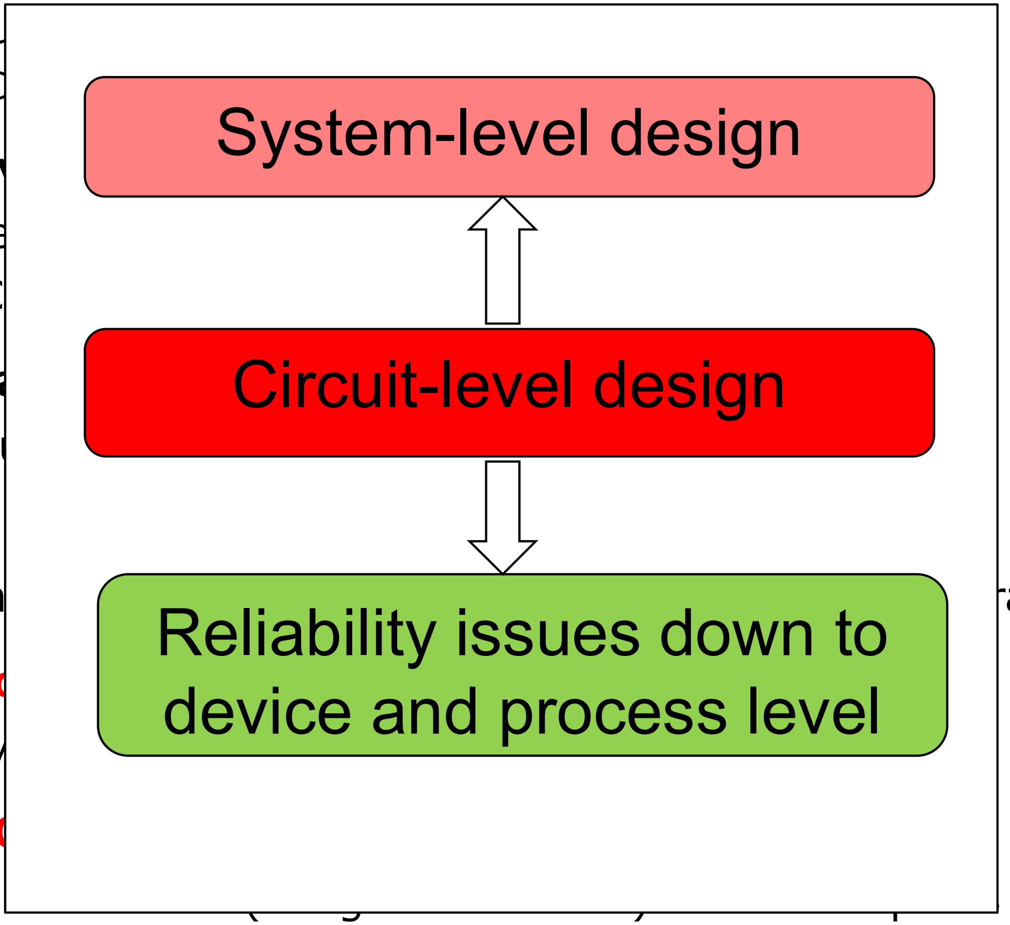
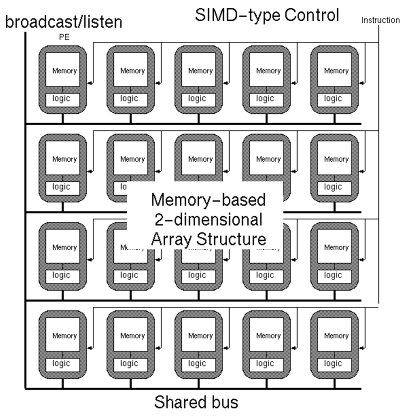
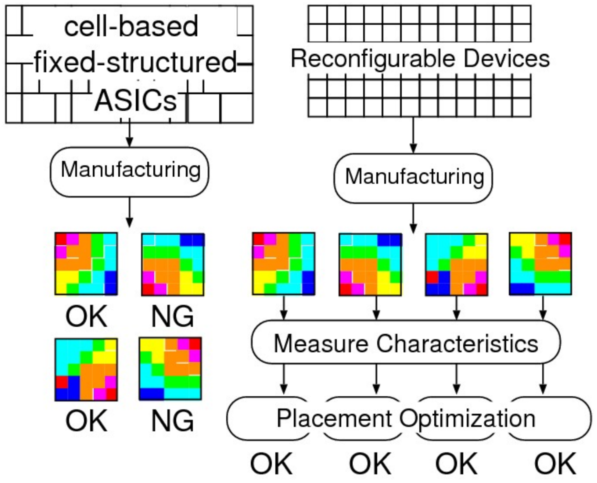




FMPP



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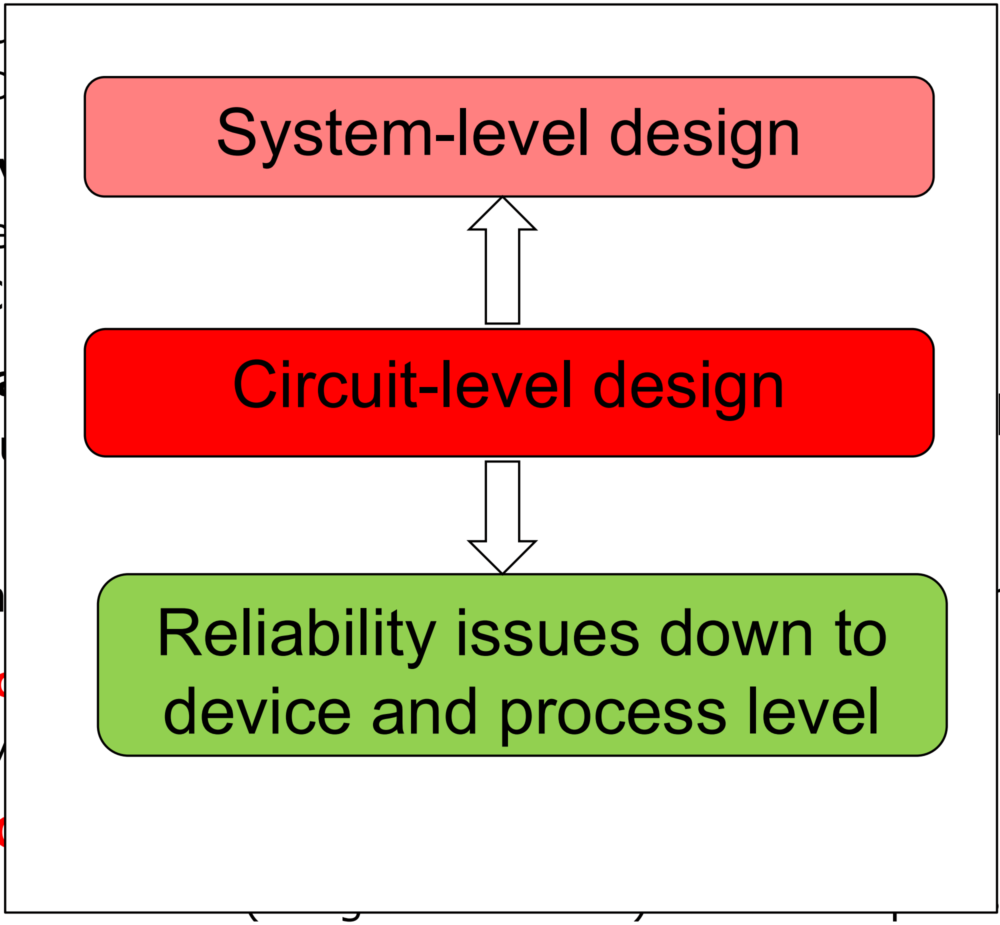
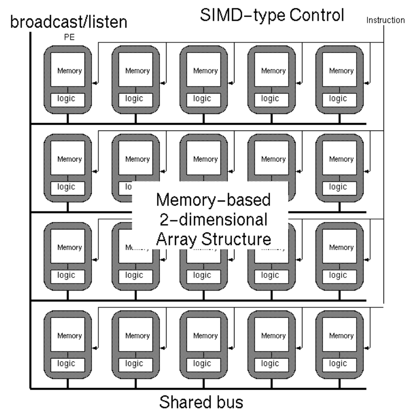
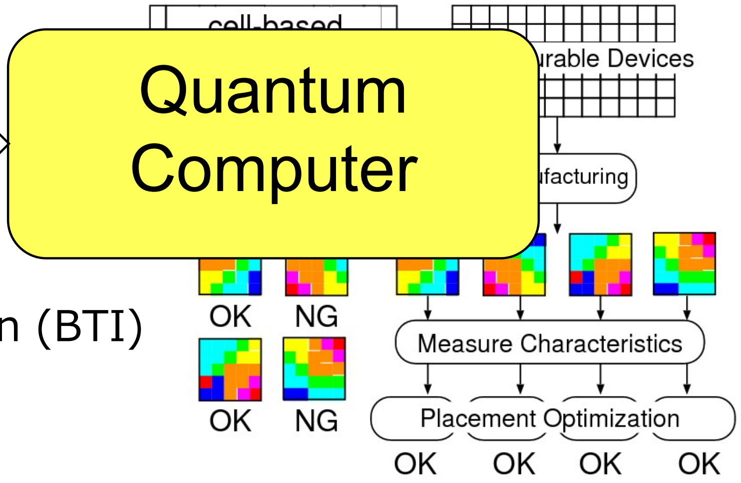




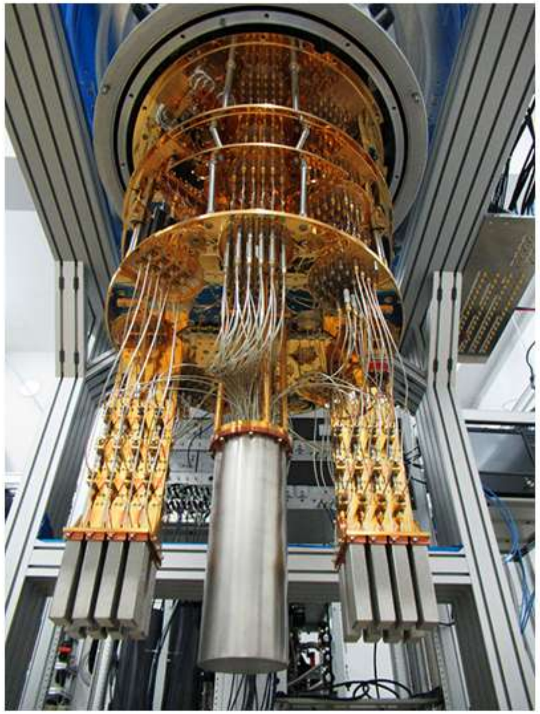
FMPP



Variation-aware FPGA

What is Cryogenic?

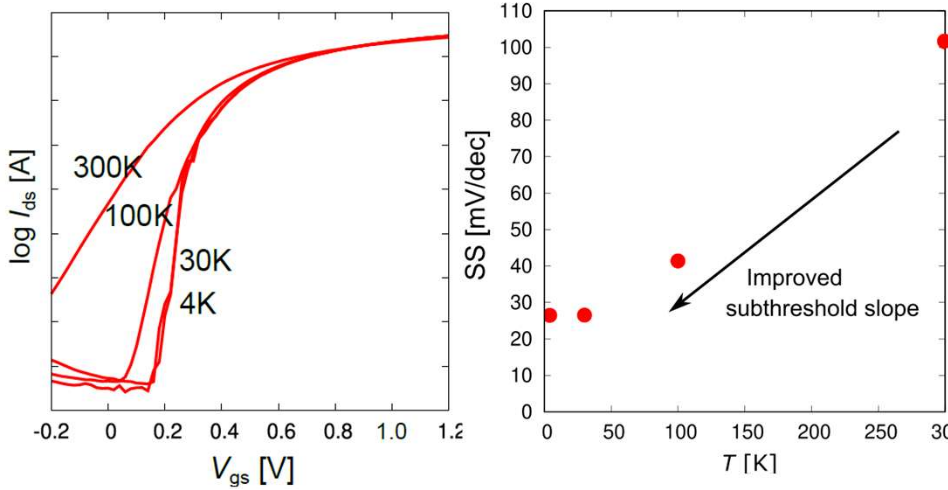
- **Answer from Google Gemini**
  - ✓ What is considered a cryogenic temperature?
    - ➢ While there isn't one universally agreed-upon exact temperature, the cryogenic temperature range is generally defined as below -150°C (-238°F). Some sources might specify slightly different thresholds, but this provides a good general understanding. This range extends down to absolute zero, which is -273.15°C (-459.67°F or 0 Kelvin), the theoretical point at which all molecular motion ceases.
- **Typical temperatures: -196°C (77K) by liquid Nitrogen, -269 °C (4K) by liquid Helium, 10mK by dilution refrigerator**



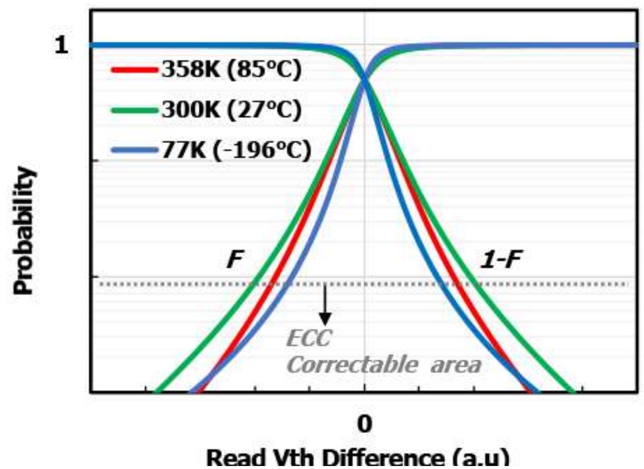
Dilution Refrigerator

Cryogenic Compute

- **Higher Vth(lower leakage), lower noise**
- **For HPC**
  - ✓ LTLT: Low Temperature Logic Technology (DARPA)
  - ✓ 6bit/cell NAND Flash Memory (Kioxia)
- **For aerospace, MRI**
- **For quantum computers**
  - ✓ Classical electronics to control qubits at cryogenic temperature
  - ✓ Gain Cell DRAM can replace SRAM at cryo. temp.[Poster 7, Cool chips 28]



[M. Shintani et.al, ASP-DAC 2025]



[Y. Aiba et.al, EDTM2021]

Governmental Funds and Projects to Support QC

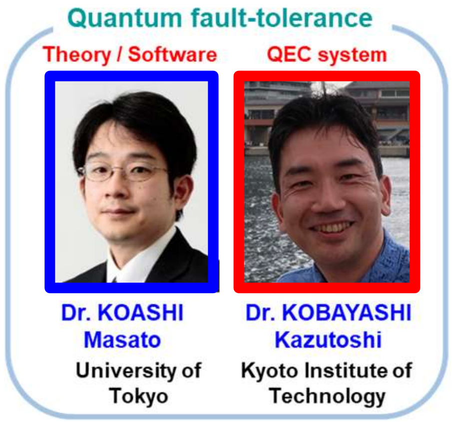
- **Q-LEAP (Quantum Leap Flagship Program) 2018-2028 https://www.q-leap.org/**
  - ✓ Deal with broad area of quantum technology including quantum computers
  - ✓ Prof. Nakamura (Riken) and Prof. Fujii (Osaka-U) are project leaders of hardware and software
- **Q-STAR (Quantum STrategic industry Alliance for Revolution) 2021 https://qstar.jp/**
  - ✓ Accelerates the shift to quantum technology through industry-government-academia collaboration
  - ✓ 17 Special member companies: KYOCERA, Canon, NEC, Hitachi, Fujitsu, Fixstar, Toyota and etc. Many corporate and start-up members
- **Moonshot Goal 6, 2020-2030 https://www.jst.go.jp/moonshot/en/program/goal6/**
  - ✓ Only focus on FTQC

Moonshot Goal 6 "Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050."

List of Project Managers

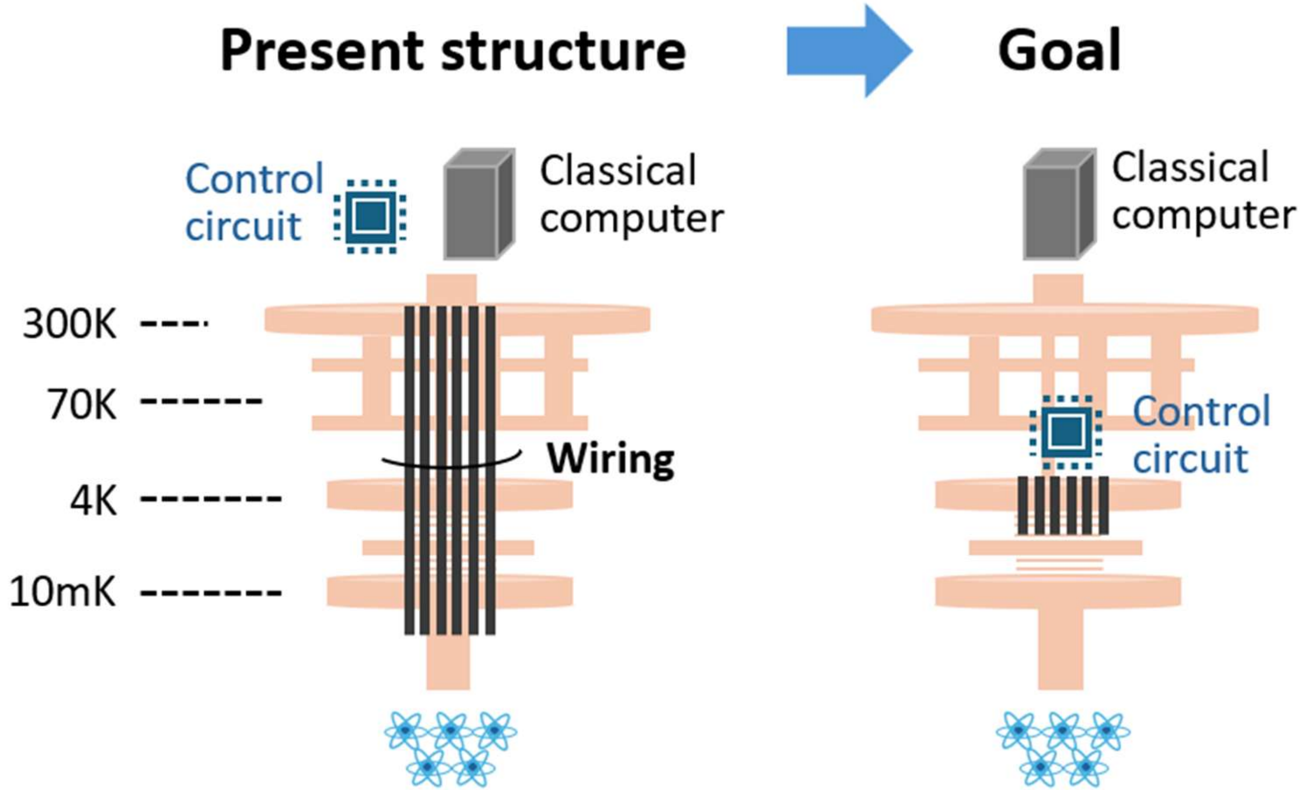
Program Director
Prof. Kitagawa
(QIQB, U Osaka)

- **7 project managers (PMs) 2020-2025**
  - ✓ 5 PMs joined in 2022
- **PMs will be renewed from 2026**
  - ✓ 12 PMs to ~8 PMs
    - ➤ 1 PM for each qubit



Development of Scalable Highly Integrated Quantum Bit Error Correction System (QUBECS)

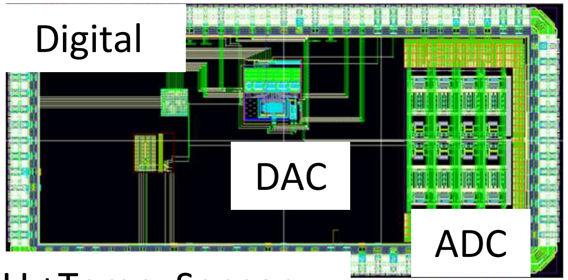
- **Cryo CMOS is used to control qubits to reduce heat dissipation from 4K stage and to increase # of controlled qubits.**
- **Ultra low-power is mandatory. Power budget at 4K stage is around 1W.**



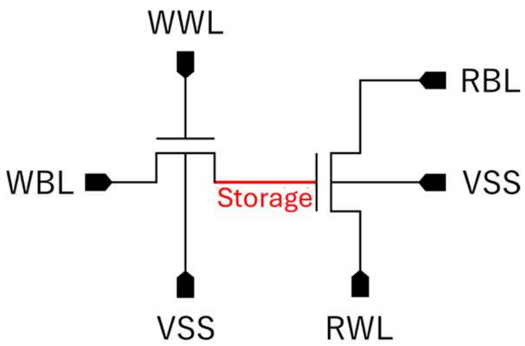
Superconducting Qubits

Cryogenic CMOS to Control Qubits in QUBECS

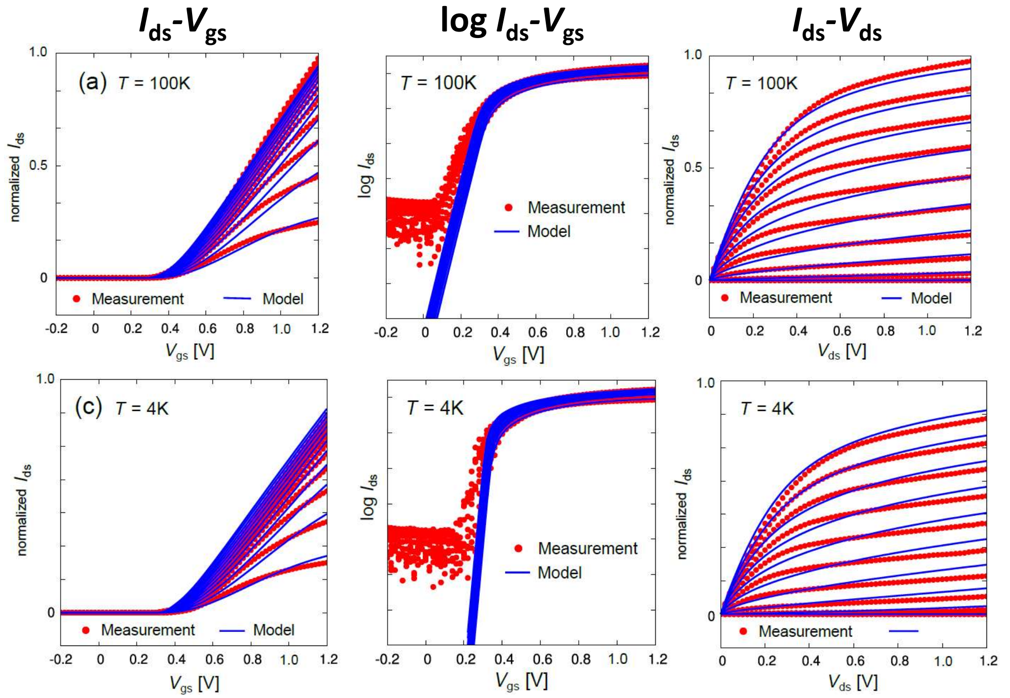
- Cryo CMOS Model [M. Shintani et.al, ASP-DAC 2025]
- Cryo SoC [Not yet published]
- Cryo Gain Cell DRAM [K. Kobayashi et.al, Cool Chips 28, 2025]



Cryo SoC in 22nm



Gain Cell DRAM



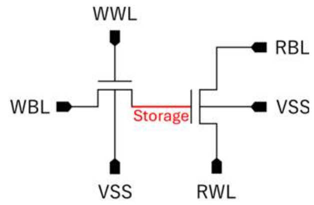
[M. Shintani et.al, ASP-DAC 2025]

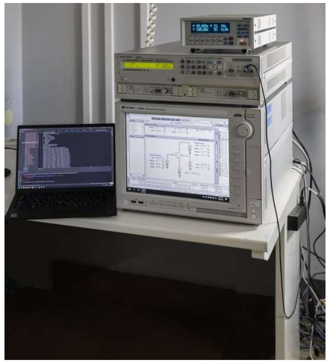
22-nm Gain Cell DRAM at Cryo Temperature

- **At 20-30K, retention time of a lvt GCDRAM cell becomes > 10ms.**
  - ✓ At RT, retention time < 10ns.
  - ✓ Over 1e6x longer at cryo temp.

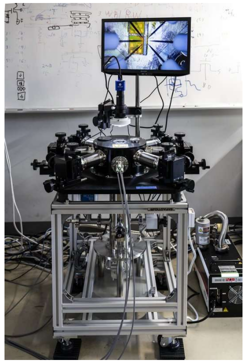
	6T-SRAM	GCDRAM
Cell area	$0.341\mu m^2$	$0.152\mu m^2$

56% area reduction



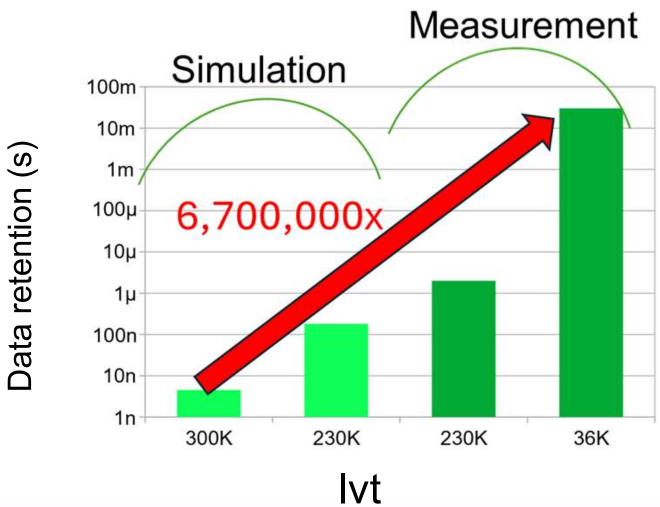


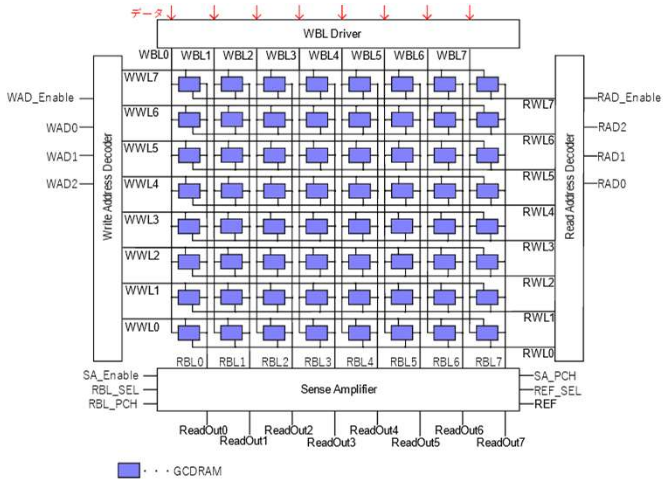
Keysight B1500



Cryo Prober

Measurement system





8wx8b DRAM Array

For temporal memory w/o refresh

Answer for the Questions

- **What is your technologies for sustainable computing?**
  - ✓ Quantum computer for true AI. Not LLM-GPU-based fake AI
    But Qubits are too unreliable.
    Classical electonics (semiconductor chips) must support qubits to control and correct errors

- **What are the synergies with other panelists?**
  - ✓ I am already involved in the quantum computer field.
  - ✓ My Ph.D. thesis was CiM in 1998. CiM rebirth to fight with GPU.
    Qubit gate operations are ultimate CiM!

Thank you!

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

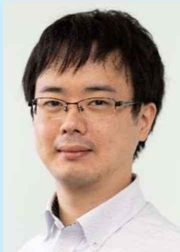


Sano
(RIKEN)

Kadomoto
(U Tokyo)

Osana
(Kumamoto U)

Subject 1: Backend for error correction




Shiomi
(U Osaka)

Shintani
(KIT)

Sato
(Kyoto U)

Matsuo
(U Tokyo)

Subject 3: Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits

Igarashi
(Socionext)

Subject 5: Frontend RF LSI at room temperature

Miyoshi
(Quel)

Subject 2: Advanced Qubit Control Frontend

Quel-1: Qubit Controller






Kobayashi
(KIT)

Tsuchiya
(Shiga Pref. U)

Takai
(KIT)

Miyahara
(KEK)

Imagawa
(Fukui U)

Kishida
(Toyama Pref. U)

Subject 4: Cryo CMOS ASICs for Frontend/backend

Principal Investigators (PIs) in QUBECS

Search “QUBECS”

Thanks!

Search “QUBECS”